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1 July through 31 December 1976

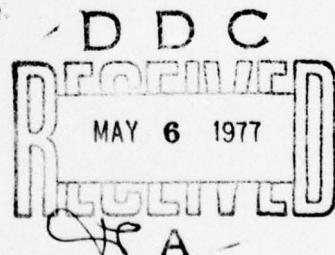
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Prepared by

Information Systems Laboratory
Digital Systems Laboratory
Integrated Circuits Laboratory
Solid-State Electronics Laboratory
Radioscience Laboratory
Institute for Plasma Research
Hansen Laboratories



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I. INFORMATION SYSTEMS

A. Project 6151. PATTERN RECOGNITION

Principal Investigator: T. M. Cover
Staff: R. King, A. El Gamal, W. Rogers, K. Jarett,
J. van Campenhout, P. Algoet

1. Objective

The purpose of this project is to investigate problems of information processing and pattern recognition.

2. Current Status of Work

a. Measurement Selection (T. Cover, J. van Campenhout)

Virtually any ordering of the probabilities of error $P(S)$ as a function of the 2^n subsets $S \subseteq \{x_1, x_2, \dots, x_n\}$ is possible. As a result, it can be demonstrated that no nonexhaustive measurement-selection procedure exists for finding the best k -element subset of measurements. This work is being extended to prove that arbitrary $P(S)$ assignments are achievable.

b. Kolmogorov Complexity and Shannon Entropy (T. Cover, C. Leung)

The Shannon and Kolmogorov notions of complexity can be shown to be essentially the same by placing the algorithmic problem of Kolmogorov in a probabilistic framework.

c. Estimating the Entropy of English (T. Cover, R. King)

A certain gambling estimate of entropy is asymptotically consistent. Experiments reveal that the entropy of English is approximately 1.3 bits per symbol, thereby indicating an achievable data compression on English text of 3 to 1.

d. Two-Way Channels (T. Cover, R. King, A. El Gamal, K. Jarett)

An attempt is being made to determine the capacity region of the Blackwell two-way channel.

B. Project 6240. OPTIMAL CODES WITH VARIABLE WEIGHT SYMBOLS

Principal Investigator: J. Gill
Staff: N. Cot

1. Objective

The objectives of this project are to determine procedures for producing optimal uniquely decipherable codes, using symbols of unequal costs, and to study the properties of optimal codes.

2. Current Status of Work

We have demonstrated that variable-length coding schemes have applications in several fields other than communications. These include

- (a) game theory where they are associated with the determination of optimal gambling strategies
- (b) data allocation in storage and data retrieval [1] where their application is based on the relationship between double-chained trees and variable-length codes; a file can be organized as a double-chained tree in which keys correspond to variable-length code words

In (b), an optimal tree (or code) corresponds to a minimal average search time. If $0 < b_1 < b_2 < \dots < b_t$ are the costs of the symbols of a code alphabet and if λ is determined by

$$\lambda^{-b_1} + \lambda^{-b_2} + \dots + \lambda^{-b_t} = 1$$

then the converse to the source-coding theorem provides a lower bound on the average cost \bar{c} of a code $\{w_1, \dots, w_n\}$ with code-word probabilities (p_1, \dots, p_n) :

$$\bar{c} \geq \frac{H(p_1, \dots, p_n)}{\log_2 \lambda}$$

where $H(p_1, \dots, p_n)$ is the entropy in bits of the probability distribution p_1, \dots, p_n .

We have established an upper bound on the cost of optimal codes,

$$\bar{c} < \frac{H(p_1, \dots, p_n)}{\log_2 \lambda + b_1 + \delta}$$

where $\delta \leq b_t$ is a quantity calculated from the costs b_1, \dots, b_t . Using this upper bound, we can efficiently find nearly optimal codes for unequal probabilities.

For equiprobable code words, a procedure [2] for producing optimal codes has been analyzed and shown to require $O(\log^t n)$ steps to produce an optimal code with n code words. Current research deals with extending this procedure to nearly equiprobable code words.

References

1. L. Stanfel, "Optimal Trees for a Class of Information Retrieval Problems," Info. Stor. Retr., 9, 1973, pp. 43-59.
2. N. Cot, "The Complexity of the Variable-Length Encoding Problem," Sixth Southeastern Conference on Combinatorics, Graph Theory, and Computing, 1975.

C. Project 6302. PROBLEMS IN CONTROL

Principal Investigator: G. F. Franklin
Staff: G. Aral

1. Objective

This study is concerned with design problems in automatic control systems, especially when model uncertainty is present.

2. Current Status of Work

An interpreter in APL language has been developed for linear control design problems. This system

- allows incorporation of new routines in a trivial way

- is flexible enough to accommodate a wide range of user familiarity with the system, allowing use of its functions in either a user-passive or user-active manner

This transition in mode is not abrupt in that the user can be as active as his knowledge of the system permits. An intensive user can reduce terminal time as he becomes more familiar with the system, and a one-time user does not require a detailed study of function descriptions.

The following features of APL make it attractive as an interpreter language.

- It is designed as an interactive language.
- This language has powerful algebraic and string-handling functions.
- The file system and storage capacity are extensive.

The three types of functions that form the interpreter are design, system, and internal functions. Internal functions are hidden from the user and are virtually inaccessible. Design and system functions are niladic and act on predetermined global system variables. All actions of the system follow three steps:

- possible modification of the content of the global system variables to be used by the functions
- execution of specified function(s)
- possible transfer of the content of the global system variables that contain the results of the executed function(s) into prescribed global user variables

All the commands entered by the user are analyzed and separated into a function name, a separator, and a parameter set. The separator is either a blank or dot; for example,

```
SAMPL  
SAMPL F,G,DELTA,PHI,GAMMA  
SAMPL .
```

where SAMPL is a function name, and F,G,DELTA,PHI,GAMMA is the parameter set.

If the separator is a blank and the parameter set is empty, the system operates in the passive mode and guides the user to provide the necessary information by requesting data input or global user variable names containing the data and requesting the output medium as a global user variable name or display. If the separator is blank and the parameter set is sufficient, the contents of the given input variables are transferred to the global system variables, the function is executed, and the results are transferred from global system variables to the corresponding global user variables. If the separator is a dot, the system executes the named function with the current content of the global system variables and outputs the results to the global system variables.

The following features of the system are a great convenience.

- The user can set up and execute sequentially a given list of commands.
- A multilevel activation of the system is allowed so that, while the system is active, a new system can be activated which suspends all the global system variables of the initial system and creates a second generation of global system variables.

The number of activated levels is restricted only by the memory of the computer. Return to the upper level system destroys the global system variables of the lower level system.

Design and system functions are incorporated into the system. The addition of many other functions is the result of user request and programmer effort.

D. Project 6418. OPTICAL COMPUTATION BASED ON RESIDUE ARITHMETIC

Principal Investigator: J. W. Goodman
Staff: A. Huang

1. Objective

Since 1 October 1976, this project has been reactivated. Its new goal is to explore the feasibility of realizing an optical computer based on residue arithmetic.

2. Current Status of Work

Arithmetic operations based on a residue number system have the fundamental advantage of not requiring carries between adjacent columns. Operations can be performed in parallel channels, with no need for one channel to wait for the result of operations performed in another channel. The inherent parallelism of these operations, plus the well-known capability of optical systems for operating in many parallel channels, has stimulated interest in the possibility of an optical computer based on residue arithmetic [1].

If the value of a number is represented by the spatial location of a small spot of light, the operations of residue conversion, addition, subtraction, multiplication, and return to a mixed radix system can be performed by certain elements called "maps" that change the spatial location of the spot in accord with the operation to be performed. The basic components of an optical residue computer, therefore, are prearranged elements that map a set of possible input spot locations into a set of output spot locations and a device that selects between the various mapping elements. To add two numbers, the first number is represented by the spatial position of a light spot, and a map corresponding to addition by the second number is selected. The position of the output light spot represents the result of the computation.

An arithmetic unit based on these principles has certain attractive properties above and beyond the potential speed resulting from the parallelism of the computations. First, the accuracy of computations can be increased simply by adding new modules in parallel; second, the computer is highly fault tolerant, with accuracy degrading slowly with internal defects rather than failing catastrophically.

During the past few months, we have examined a variety of technological approaches to realizing the maps and selectors; however, the ideas for organizing and structuring the mapping operations are evolving too rapidly for us to select one particular technological approach. Accordingly, current work is concentrated on improving the architecture envisioned for the optical computer.

Starting in February 1977, this work will be supported by a contract from the Air Force Office of Scientific Research, and the current JSEP project will be terminated.

Reference

1. Alan Huang, "The Implementation of a Residue Arithmetic Unit via Optical and Other Phenomena," Proc. of the 1975 International Optical Computing Conference, Apr 1975.

E. Project 6503. DATA COMPRESSION TECHNIQUES AND APPLICATIONS

Principal Investigator: R. M. Gray
Staff: Y. Linde

1. Objective

Our goals are to develop the theory and computer-aided design techniques for nearly optimal data-compression algorithms.

2. Current Status of Work

With the joint support of JSEP and AFOSR, a simulation capability for trellis coding was developed on the Information Systems Laboratory Interdata 7/16 computer. Numerous simulations were conducted for compressing binary and gaussian sources with memory. Decoders for binary sources were searched exhaustively up to length four. Decoders for gaussian sources were selected via ad hoc techniques, particularly by similarity to predictive quantizer decoders and from Central Limit Theorem arguments. The gaussian codes performed approximately 1 dB better than traditional DPCM techniques and suggested some additional methods that should produce even better performance. The binary codes did not yield insight into good code design, and further work is necessary. Because the Interdata computer is now gone, some time will be required to adopt the programs to the new computer, and then the simulation studies can be continued. In the meantime, our focus will be directed toward analysis of the newly developed coding structures.

F. Project 6601. INFORMATION THEORY AND INFORMATION PROCESSING

Principal Investigator: M. E. Hellman
Staff: L. Pinto de Carvalho, R. Kahn

1. Objective

The objective of this project is to investigate the relationships between information theory, information processing, and complexity theory.

2. Current Status of Work

Coding schemes for the wiretap channel with feedback are being considered. A trade-off between entropy production (to confuse the wiretapper) and information flow has been established. This trade-off and recent results from other multiuser communication channel models are being studied for use in bounding the achievable rate-equivocation region.

G. Project 6701. ADAPTIVE FILTERING

Principal Investigator: B. Widrow
Staff: C. Williams, M. Larimore, J. Treichler

1. Objective

The objective of this project is to study the effectiveness of various adaptive techniques in digital communication systems. Interest has focused on adaptively computed direct-channel models in systems where doppler effects, multipath, and additive noise are present. Other work is concerned with the application of adaptive techniques to the detection of spectral lines in noise.

2. Current Status of Work

The study of adaptive channel modeling in the presence of doppler and/or clock asynchronization is continuing in a new direction. We have obtained a good characterization of the LMS-driven adaptive model performance and are now investigating schemes for augmenting the algorithm

to improve its asynchronous performance. These schemes are divided into (a) adaptive techniques for adjusting the receiver clock based on model behavior and (b) techniques for augmenting the algorithm to include an adaptive correction in the channel model. This line of research is new and appears to be promising.

The extraction of a narrowband signal buried in noise is one of the oldest, yet still important, problems in the areas of communication and signal processing. We are continuing our development of the adaptive line enhancer (ALE) to separate a signal into its narrow- and broadband components. A conclusive study of the line enhancer, using an all-zero (feedforward) adaptive filter, has been completed. We are now investigating a line enhancer that employs a feedback and feedforward ("poles" and "zeros") adaptive filter. The poles provide a high "Q" filter with a small number of adaptive weights and, thereby, is highly suited for the detection of narrowband signals buried in noise. The operation of the adaptive feedback filter is significantly more involved than that of the feedforward filter and is, of itself, a research topic. Our preliminary results indicate that the feedback line enhancer is a great improvement over the feedforward device.

H. Project 6851. IMAGING OF GAMMA-RAY DISTRIBUTIONS

Principal Investigator: A. Macovski
Staff: A. L. Steinbach, D. Rosenfeld

1. Objective

The objectives of this work are to study the fundamental characteristics of a gamma-ray source distribution and to derive optimal methods for imaging such distributions. Because refractive effects do not exist at these energies, various attenuative masking structures are being investigated with respect to efficiency, resolution, depth delineation, and signal-to-noise ratio.

2. Current Status of Work

This represents the conclusion of work on this project. Two doctoral dissertations are being prepared. They will describe the use

of zone plates and modulated apertures to efficiently image gamma-ray sources.

In the work based on zone plates, the three-dimensional point response of the entire system has been analyzed, including encoding and decoding. The output of the computer plotter graphically demonstrates system performance, including lateral and depth resolution and sidelobe response. Several zone-plate configurations have been studied to determine those that provide the best performance in various dimensions. Apodization has been investigated as a trade-off between the size of the central lobe and the amplitude of the sidelobes. The results provide a wealth of design criteria for these structures.

In the work using modulated apertures, many computer simulations and analytical studies have been performed. The analyses have demonstrated that the resultant reconstruction is optimum in the maximum likelihood sense. A method has been derived to determine the optimal code parameters for a given object size; this code parameter represents the number of imaging apertures open at any given time period of the code cycle. Several codes have been considered and implemented. A number of criteria have been used, including maximizing the maximum signal-to-noise ratio in the image or maximizing the minimum signal-to-noise ratio. A simulated reconstruction of a three-dimensional object, in the presence of counting noise, is under way to indicate the ability to separate planes in space.

I. Project 7050. STUDIES IN STATISTICAL SYSTEM THEORY

Principal Investigators: T. Kailath, M. Morf
Staff: J. Dobbins, B. Levy, S-Y. Kung, E. Verriest,
A. Vieira

1. Objective

The purpose of this project is to study basic problems in statistical system theory.

2. Current Status of Work

a. Square-Root Algorithms for the Continuous-Time Linear Least-Squares Estimation Problem (M. Morf, B. Levy, T. Kailath)

We have found a simple differential equation to propagate the triangular square root of the error covariance of the linear estimate of the state. This differential equation does not involve the antisymmetric matrix which appeared in the previous work of Andrews and Tapley and Choe. We combine both results by constructing an explicit antisymmetric matrix that generates the orthogonal transform that continuously triangularizes the square-root factor.

As in the discrete case, an array method for handling the continuous square root was developed and yields the usual normalizations of stochastic calculus and the results of the other approaches. In the constant model case, it is demonstrated that the Chandrasekhar equations are a set of square-root equations for the derivative of the error variance.

b. Multichannel Maximum Entropy (M. Morf, A. Vieira, T. Kailath)

Our work on multichannel maximum entropy methods (MMEM) is progressing. A paper has been completed and has attracted considerable interest. Pusey (at EXON) has implemented our algorithm in the computer and verified the expected well-behavior of the numerical properties. The derived spectral estimates appear to be very close to the maximum likelihood estimates (quote from F. Muir, EXON, a frequent guest in the Stanford Geophysics Department). An invitation has been extended to Professor M. Morf to present a paper on this subject at the 1977 JACC Conference in San Francisco to a special topics session on geophysical data processing organized by J. Mendel (USC).

c. Ladder Structure for Least-Squares Estimation
(M. Morf, A. Vieira, T. Kailath)

Ladder structures increasingly appear to be the "natural" canonical form for estimation problems. We have developed exact least-

squares recursions for such relations (including multidimensional versions) and have found that they have even less computations and storage requirements than our earlier forms of fast algorithms for linear prediction.

These recursions do not require "auxiliary" variables as did the earlier forms, except for a set of scalars that perform the function of "optimal weights" in real-time correlators that compute the model parameters. In a project on speech processing, we have written a survey paper in which some of these new results are included. They will be extremely useful in that project because they will be part of a set of fast and efficient speech-encoding algorithms for high quality and low data-rate properties. A more extended version of this paper on scalar ladder forms is planned for the IEEE-ASSP Journal and a multi-channel version for the IEEE-AC Journal.

d. Square-Root Algorithms for Model Sensitivity Analysis
(M. Morf, T. Kailath, J. Dobbins, E. Verriest)

We have developed square-root algorithms for calculating the true error covariance of a Kalman filter estimate based on an incorrect model of the process under observation. These algorithms have been extended to the smoothing problem. When based on an incorrect model, the filter arrays do not properly orthonormalize the estimate residuals. Our algorithms propagate on additional arrays that complete the orthonormalization.

We are applying these methods to the singular perturbation problem. Work is also progressing on connecting the successful square-root and scattering-theory frameworks for least-squares estimation.

e. Minimal Partial Realizations of MIMO Systems
(S-Y. Kung, T. Kailath, M. Morf)

We have demonstrated that a modified Lanczos recursion can be used to attain a minimal partial realization of SISO linear systems. The first step is to define a Hankel matrix $H = [h_{i+j}]$ where h_{i+j} is the $(i+j)^{th}$ Markov parameter. The key step is to transfer this

Hankel matrix into an echelon matrix until a dependent column is obtained. The denominator of the solution is then solved by noting that its coefficients are simply those dependent coefficients of the dependent column. This procedure guarantees that the order of our solution system (say n) is indeed a minimal one.

We will extend the above recursive algorithm to the MIMO partial realization problems. A pseudo-canonical polynomial matrix is first introduced. This Popov form has an indispensable structural property and very powerful applications in many design problems in addition to the partial-realization one. Our procedure is again to transform the Hankel matrix into an echelon form and to find m (where m is the number of inputs) primary dependent columns. It can be shown that this procedure guarantees a set of minimal input dynamical indices (controllability indices) and, accordingly, a minimal order of the solution system.

f. New Results on Two-Dimensional Systems Theory
(B. Levy, S-Y. Kung, M. Morf, T. Kailath)

In recent years, linear system theory has been applied intensively to estimation and control problems. At the same time, image processing has attracted increasing interest. As a result, attempts have been made to extend the techniques of systems theory to two-dimensional problems either from a polynomial (input-output) or state-space (internal) point of view.

In the first part of our work, we examined some new results obtained from two-dimensional polynomial matrices and have successfully extended the existing one-dimensional results on GCRD extraction, Sylvester resultants, and matrix fraction descriptions (MFD) to the 2-D matrices. Some of our results appear to be unique for such multidimensional problems as the existence of "primitive factorizations" in addition to general factorizations of the 2-D polynomial matrix.

In the second part of our work, we examined some definitions of state controllability and observability and their relationship to the minimality of 2-D systems. We have also investigated new circuit-realization methods, using a minimal number of dynamic elements and a new technique for 2-D digital-filter hardware implementations of 2-D transfer functions.

We have also examined the 2-D systems from a computer algorithm point of view. Our results include a generalization of Levinson's algorithm, finding a Hankel matrix, and developing a recursive realization algorithm given a set of Markov parameters. There are still many open problems for 2-D systems, such as stability tests, innovations representation, and Kalman filtering.

II. DIGITAL SYSTEMS

A. Project 6961. DESCRIPTION LANGUAGES AND DESIGN FOR GENERAL PURPOSE COMPUTER ARCHITECTURES

Principal Investigators: M. J. Flynn,
W. M. vanCleempur

Staff: T. Bennett, D. Hanson, J. Hupp, R. Lee,
K. Stevens, S. Wakefield

1. Objective

The purposes of this study are to develop description languages to describe computer architectures and to establish a basis for understanding the limits of computer-architecture design (to determine the fastest speed for the execution of a program).

2. Current Status of Work

a. Evaluation of Existing Hardware Description Languages (D. Hanson, W. vanCleempur)

To evaluate the feasibility of describing computer architectures by means of a hardware description language, several of these languages were studied. From a large number, three were selected based on the availability of a working compiler and simulator and on the suitability of the language for multilevel description of digital systems. Compilers for the CDL (Chu, University of Maryland) and the CASSANDRE (Mermet, University of Grenoble, France) were implemented, and these languages were studied and compared in terms of their descriptive power. A compiler for the DDL (Dietmeyer, University of Wisconsin) was obtained and is being adapted for the IBM 370 system.

b. Development of a Structural Description Language (W. vanCleempur)

Most of the existing hardware description languages emphasizes a behavioral description and neglects the structural aspects of a design. A behavioral description is often more than sufficient to describe an existing architecture; however, to aid in the design process, it is necessary to capture all available information--structure as well

as (intended) behavior. The SDL language was developed to describe accurately the structural properties of the system, and a compiler is currently operational. A special characteristic of the SDL is that it is hierachial in nature.

c. Applications of the Structural Design Language
(T. Bennett, J. Hupp, K. Stevens, W. vanCleempunt)

One application of a structural design language is to serve as the input medium for a physical design system. Such a system may consist of several subsystems to perform such tasks as printed-circuit layout, integrated-circuit layout, gate-level logic simulation, circuit-level simulation, fault test generation, and automated logic diagram generation. A printed-circuit layout system is being implemented, and a prototype will soon be operational. An integrated-circuit layout system is in the design phase. Interfaces between the SDL language and several existing logic- and circuit-level simulators are in the planning phase.

d. Bounds for Maximal Parallelism (R. Lee, M. Flynn)

This is a study of the performance limits of a single program executed on a large number of identical processors operating in parallel in an MIMD (multiple instruction multiple data) organization. With the rapidly decreasing cost of LSI microprocessors, it is now economically feasible to consider an army of processors within the computer architecture to speedup a computation, even at reduced efficiency of each component processor. No longer is the processor the hallowed CPU (central processing unit) or the most valuable resource to be utilized with the greatest efficiency. Some "acceptable" level of efficiency should be obtained, however, but we must determine what type of speedup can be expected by increasing the number of processors even if we ignore the problems of control and communication that accompany the cooperation and competition between these processors.

We first defined a general model computation on a p-parallel processor, distinguishing clearly between the logical parallelism (p^* processors) inherent in a computation and the physical parallelism

(p processors) available in the computer organization. We then determined such performance measures as execution time, speedup, efficiency, and space-time product by which we could evaluate the performance improvements (if any) of p -parallel processor systems over uniprocessor systems. The results obtained indicated that, generally, performance depends on both the computer architecture and the computation.

We then derived necessary and sufficient conditions for the maximum attainable speedup of a p -parallel processor over a uniprocessor to be $S_p \leq \min(p/\ln p, p^*/\ln p^*)$. Despite the many different views concerning the potential speedup of parallel processor systems, this bound has never before been established.

In addition, if there are always sufficient processors ($p \geq p^*$), conditions can be derived under which the maximum attainable speedup of a computation is $p^*/\ln p^*$, maximum efficiency is $1/\ln p^*$, minimum execution time is $T_1 \times \ln p^*/p^*$, and minimum space-time product is $T_1 \times \ln p^*$ (where T_1 is the execution time of the computation on a uniprocessor). In fact, the empirical speedups obtained for a large number of different computations indicated that 80 percent of all programs examined satisfied these conditions and had maximum speedups of less than $p^*/\ln p^*$.

e. Parallel Information Processing in Biological Systems
(S. Wakefield, M. Flynn)

The interconnections and types of synapses between units of a particular neural subsystem (the stomatogastric ganglion of the lobster) have been determined by biologists, as have the stereotyped motor patterns that it produces; however, the exact mechanisms and sequence and duration bounds of impulse bursts that must underlie the production of the coordinated muscle-activation patterns are unknown. Such a mechanism would be analogous to the switching network responsible for the traversal of states in a digital sequential circuit. Because of this analogy, this and similar simple biological information-processing subsystems are being investigated. In addition, the speed, power requirements, size, information capacity, and other characteristics of individual neurons are being compared to those of electronic information-processing components.

B. Project 7151. COMPUTER ARCHITECTURE

Principal Investigators: E. J. McCluskey,

S. S. Owicki

Staff: J. Losq, R. C. Osgus, D. J. Rossetti,

A. Spector, F. W. Terman

1. Objective

The objective of this study is to gain new insight into computer architecture and operating systems. We intend to design a small operating system and to verify its correctness. Another goal is to develop new methods to evaluate system performance and to use the results obtained for better system design.

2. Current Status of Work

This project has developed in two major directions--an investigation of operating-system correctness and the development of analytical models and monitoring systems for performance evaluation.

The basic methods for designing and verifying the correctness of concurrent programs have been analyzed. The design of a probably correct operating system is under way, and the high-level description is nearing completion.

A set of trace programs has been developed to measure microprocessor performance and to provide unique information concerning the programming ease of various microprocessors. The tracing is highly powerful (can record interrupts and I/O behavior) and almost transparent (external hardware reduces significantly the amount of perturbation introduced by the tracer).

The investigation of interleaved memory is being extended to the effects of request ordering and to the most efficient ordering. A new model has been developed to evaluate the performance of gracefully degradable multiprocessor systems, based on such measures as availability, processing power, and proportion of time in the degraded mode. It also allows one to determine the best trade-off between computing power and availability or between hardware vs software fault detection.

A new testing method indicates that random inputs can be used efficiently to test sequential circuits. A statistical analysis revealed

that this method is potentially the most cost effective for in-the-field testing.

a. Specification and Verification of Monitors (S. Owicky)

A monitor is a programming language construction that defines a logically related group of shared data items and a set of operations on those items. The operations are the only means by which programs may access the shared data, and the monitor includes synchronization to ensure that processes do not interfere with each other as they perform their operations. This limited access simplifies the verification task.

A monitor is specified by listing the shared data items, their initial values, and the effects of each operation. Verification of programs is simplified by describing the operations in terms of variables that are private to the program invoking the operation. The relationship between the private and shared variables is expressed by an invariant relation, which is true for the initial monitor values and is preserved by each operation.

There are two steps in the process of verifying systems that use monitors. The first shows that the monitor satisfies its specifications (that the operations preserve the invariant and have the required effect on the private variables), and the second verifies the processes that call the monitor by using the specifications of the monitor operations. In some instances, the correct behavior of one process depends on the actions of another. Here it is convenient to use a process invariant--an invariant relation on the private process variables. These tools appear to be powerful enough for most applications of concurrent programming with monitors. Further work is required to develop methods for treating dynamically allocated resources that do not fit the monitor pattern.

b. Operating System Design (A. Spector)

Our work has focused on the design of a paging interactive time-sharing system suitable for a computer such as a PDP11/70. Although we do not expect to include very complex I/O or protection mechanisms, we are attempting to develop a realistically usable system.

The system will be a hierarchy consisting of two levels--the kernel and the supervisor. The kernel is the more primitive run-time support system that implements the basic operations of the high-level programming language used by the supervisor. More specifically, it contains the machine-dependent operating-system independent procedures that provide concurrent processes and monitors. It also translates certain privileged hardware operations to language-level primitives. For example, because supervisor processes use monitors to communicate, the kernel must maintain the queues necessary to support critical sections and wait and signal primitives. An unusual feature is that the kernel maintains detailed per-process state information that can be used by such supervisor routines as scheduling and accounting.

Although the nucleus is small and can be thought of as a single entity, the supervisor performs many complex functions and is best considered as a hierarchy. For example, the long-term process scheduler is a primitive operation of the supervisor and underlies the operation of the whole system. Our design calls for this process to run synchronously and to communicate periodically to the kernel a set of processes that can be executed in some ensuing interval. The memory allocation process (also one of the basic operations) contains the logic to allocate physical memory to processes and to support shared and nonshared pages. Scheduling and memory-allocation decisions can be made with the use of state information recorded by the kernel and from information contained in certain supervisor monitors. Higher levels of the supervisor hierarchy include sections to support I/O and user program calls.

During this reporting period, our work has focused on the design of the most primitive portions of the system. We believe that such issues as the accurate assignment of meanings to language primitives and the proper definition of the boundary between the kernel and supervisor will greatly influence the outcome of our project. As a result, we are proceeding with caution in the hope of preparing a sound basis on which to construct a carefully structured and verified system.

c. Trace Facility (D. J. Rossetti)

The STRAP/370 instruction tracing facility described in previous reports is providing data for various studies in the areas of

performance, architecture, and operating systems. A paper entitled "The Design and Implementation of an Operating System Tracer" has been submitted for publication in the Communications of the Association for Computing Machinery. It describes the unique aspects of the tracer, provides some examples of its use, and recommends further applications of the data and the technique.

Our approach is being extended into the microprocessor area, retaining most of the desirable features of the original technique. The purpose is to evaluate computer architectures from the standpoint of development and programming ease as opposed to processing speed because software development has become a major cost in microprocessor use. The principal tool is a detailed level instruction tracer having the following characteristics.

- It is independent of the program being measured to the extent that one microprocessor can be used to measure another.
- The instruction stream is sampled in bursts at a rate determined by the user.
- Minimal perturbation is introduced into the measured system because the trace is collected with hardware assistance and not by interpretation.
- Actual systems and programs can be measured, including I/O and interrupts; the trace is not gathered in an artificial environment, such as a simulator.

The tracer has been used to gather instruction frequency data for application programs in our microprocessor laboratory. Current plans are to collect extensive trace data for studies in architecture evaluation and to gain understanding of microprocessor program and input/output behavior.

d. Memory Interleaving (F. W. Terman)

A series of models of interleaved memory systems has been investigated by means of a trace-driven simulation. The basic model extends the one developed by Burnett and Coffman [1] to the architecture of the IBM 360/370 with its variable-length instructions and operands;

it also includes multibyte transfers per memory access. Variations of the basic simulation model facilitates study of the effects of channel interference, data request reordering, and data queue emptying.

Memory requests for the simulation are obtained from two sets of instruction-by-instruction trace records. The first set, produced by the program TRACE/360 written by Terman, traces the problem state component of typical programs running on the IBM 360/370. The second set, produced by the program STRAP/370 written by Rossetti, traces samples of the total activity of the CPU, including both supervisor and problem states.

The theoretical predictions of Burnett and Coffman for the increase in memory bandwidth caused by interleaving are found to fit well with the simulation results obtained for the fetching of instructions. The usefulness of fetching instructions in blocks is limited by the relatively high frequency of branches on the IBM 360/370 machines. Consequently, an active channel has relatively little effect (less than 10 percent degradation) on the fetching of instructions from an interleaved memory.

For the transfer of operands to and from memory, the simulation results reveal only one-half the increase in memory bandwidth predicted by the analysis of Burnett and Coffman. This indicates that data references on the IBM 360/370 are not random as were assumed. The effect of an active channel is again small because of the number of idle modules in a typical memory cycle. A larger degradation (10 to 20 percent) occurs if the data requests are forced to "catch up" with the instruction requests before a successful branch is executed. This is a reasonable restriction because the branch address cannot be calculated with certainty until the values of the general-purpose registers are known. On the other hand, a significant improvement (15 to 30 percent) in the memory bandwidth can be obtained by allowing the data requests to be filled out of order. These effects are being analyzed in detail and compared to the predictions of other theoretical models.

This investigation is being extended to include the effects of interference between multiple CPUs. The effects of the interdependencies between instructions and operands and between the operands themselves will also be examined.

e. Gracefully Degradable Systems and Their Performance
(J. Losq)

The recent development of multiprocessor systems that offer tolerance to failures by switching to a degraded mode of operation following failure occurrences has the vast potential of providing large processing power coupled with high reliability (availability). A general model has been developed [2] to evaluate the performance of such systems. It takes into account the architecture of the hardware, characteristics of the various fault detection and recovery mechanisms, unreliability of the hardware components, and failure rate of the operating system. The model provides such measures of overall system performance as average processing power, mean time between crashes, and the proportion of time spent by the system in the degraded mode. The best trade-offs between high processing power and availability (or between hardware vs software fault detection) are obtained.

This model can also determine overall performance when computer systems are seen as a combination of hardware and software, and it can be applied to almost all current multiprocessors. A detailed example emphasized the large contribution of software errors to the system down time. Future work will concentrate on an analysis of a recovery strategy and on the general problem of fault-tolerant software.

f. Efficiency of Compact Testing for Sequential Circuits
(J. Losq)

Compact testing uses random inputs to test digital circuits. Failures can be detected by comparison between some statistical property of the circuit (for example, the frequency of logic 1's on the output lines) and the same property for the fault-free circuit. Although such a method is commonly used in the field, no previous study indicates its usefulness and limitations.

This investigation [3] revealed that compact testing is indeed efficient although it has some inherent limitations. Most of the failures in a sequential circuit can be detected; however, compact testing cannot fully guarantee that a circuit is fault free. Synchronization is not a major problem--any long sequence of random inputs will act as a synchronizing sequence, and most circuits can be synchronized in such a

manner in a matter of seconds. The great majority of failures inside the memory elements can be detected, even with short tests. Compact testing also detects most of the failures in the combinational parts; its efficiency is largely dependent on the test length and on the characteristics of the random-number generators.

g. Monitors for Signal Activity (R. Ogus)

Probabilistic models have been developed [4] to describe logic circuits where a probability can be assigned to a signal line to indicate that the signal is a logic "1" given the probability of the inputs of the circuit being a "1." Algorithms have been devised to derive the signal-probability expressions as functions of the input-signal probabilities. The signal probability can be used in computing the probability of detecting faulty behavior in circuits and also in the calculation of the signal reliability of a circuit (the probability that the circuit output is correct). In addition, a scheme has been described to select efficient test sets from random inputs [5]. This method measures the effect on a circuit output of exercising any particular input variable, and the inputs can be weighted according to their importance. This requires measuring both the input- and output-signal probabilities. Other uses of the measure are found in error latency studies and in system testing.

In many cases, circuits are too large to be studied analytically and, as a result, it is desirable to have a hardware monitor unit that can actually measure signal activity and display the signal probability. Two monitor designs have been proposed. The first is a simple stand-alone single-probe device that can directly measure and display the probability of a "1" on a signal line. The second would be a processor that can insert a number of probes into a circuit and measure the signal probabilities of the lines and process the information to relate to the particular application.

The first monitor has been designed, and a prototype is being exercised. The second monitor is being considered and would be implemented on an IBM System/7 computer. These tools should be useful augmentations to the other monitors described above and should prove

valuable in several applications, including test generation and actual circuit testing.

References

1. Burnett, G. J. and E. G. Coffman, Jr., "A Study of Interleaved Memory Systems," Proc. AFIPS Spring Joint Computer Conference, 36, AFIPS Press, Montvale, N.J., 1970, pp. 467-474.
2. Losq, J., "Effects of Failures on Performance of Gracefully Degradable Systems," Tech. Note No. 103, Digital Systems Laboratory, Stanford University, Stanford, Calif., Dec 1976.
3. Losq, J., "Efficiency of Compact Testing for Sequential Circuits," Tech. Note No. 104, Digital Systems Laboratory, Stanford University, Stanford, Calif., Dec 1976.
4. Parker, K. P. and E. J. McCluskey, "Analysis of Logic Circuits with Faults Using Input Signal Probabilities," IEEE Trans. on Computers, C-24, 5, May 1975, pp. 573-578.
5. Schnurmann, H. D., E. Lindblom, and R. G. Carpenter, "The Weighted Random Test Pattern Generator," IEEE Trans. on Computers, C-24, 7, Jul 1975, pp. 695-700.

C. Project 7181. THE 2000 TERMINAL COMPUTING SYSTEM

Principal Investigator: V. Cerf
Staff: W. Warren

1. Objective

A study has been undertaken to investigate the possibilities, requirements, capabilities, limitations, and advantages of a computing system serving a very large number of users.

2. Current Status of Work

Computer and communication networks linking potential users over a large geographic area make possible a computing system with an active user population of several thousand. Functional, rather than general purpose, multiprocessing may make such a system possible. It could realize a number of economies of scale and specialization and

could provide reliability through modularity and redundancy. We have investigated the fundamental architectural requirements, limitations, functional organization, and specialization of these systems, the software requirements in a network environment, and the functional characteristics of the user interface (both hardware and software).

In our investigation of system architectures feasible for use in a 2000 terminal computing system, we have selected a distributed network of fully interconnected microprocessors. The microprocessors will be individually allocated to the functional tasks of (1) terminal I/O modules, (2) common memory modules, and (3) the general-processing modules. Each module will contain local memory, processing power, and a communication interface that will provide, via micro-watt radio, a complete interconnection network [1]. This interface will handle module-module packet communications protocol based on the carrier sense multiple-access technique developed for the ALOHA system [2,3].

One feature of this system will be the fast response time seen by the terminal users. Each terminal connected to the system will have its own dedicated terminal-I/O module attending to line control, formatting, and echoing [4]. Another significant feature would be the potential for hardware reliability, implicit when multiple copies of each hardware structure exist. Such a system, with appropriately designed software, would be able to cope with the complete failure of one or more hardware modules, resulting in a minor degradation of response time as seen by the user. This type of reliability will be obtained through the same methods and techniques used by Pluribus [5]--duplication of hardware, isolation between independent hardware modules, and a software system that performs self-consistency checking and recovery.

We have investigated the problems of recovering error-free information when a faulty hardware module is detected. If an error is detected at some point during the processing of a task, it may be necessary to amputate the faulty module, reconfigure the hardware environment, and rerun the task that failed. The rapid and systematic restoration of service after an error or malfunction would be a major design goal. The state of the system (including system and user data structures that become invalid) must be restored to a previously consistent state so that the task can be run again.

A system architecture was developed [6] to permit systematic recovery after the occurrence of an error and the restoration of erroneous data. Algorithms were developed to perform state restoration, thereby guaranteeing that a computer system and its associated data bases and communication transactions will be restored to an operational state within a given time and cost bound after detection of a system failure. The model used for these algorithms provides for recovery of the program state, revoking of erroneous outputs, and restoration of external data structures.

This research considered the optimization of a specific software strategy--the rollback and recovery strategy, within the framework of a graph model of program flow that encompasses communication interfaces and data-base transactions. Algorithms were developed to optimize the placement of dynamic recovery checkpoints. A method was presented for statically precomputing a set of optimal decision parameters for the associated program model and a run-time technique for dynamically determining the optimal placement of program-recovery checkpoints.

References

1. Okano, R., "Preliminary Design Considerations for a Multi-Microprocessor System," University of Hawaii, 1974.
2. Abramson, N. "The ALOHA System," AFIPS Proc., 37, 1970.
3. Kleinrock, L., "Random Access Techniques for Data Transmission over Packet-Switched Radio Channels," Proc. Nat'l. Computer Conf., 1975.
4. Heckel, P. C. and B. W. Lampson, "A Terminal Oriented Communication System," BCC-500, Sep 1975.
5. Ornstein, S. M. et al., "Pluribus - A Reliable Multiprocessor," Proc. National Computer Conf., 1975.
6. Warren, W. A., "The Optimal Placement of Dynamic Recovery Checkpoints in Recoverable Computer Systems," Digital Systems Laboratory, Stanford University, Stanford, Calif., 1976.

III. INTEGRATED CIRCUITS

A. Project 4606. PRECISION CHEMICAL MACHINING OF SINGLE-CRYSTAL SILICON

Principal Investigator: J. B. Angell
Staff: P. Barth

1. Objective

This project was established to perfect techniques for fabricating thin films of single-crystal silicon (5μ or less), using chemical preferential etching. This work has resulted in a new dielectric isolation technique for silicon that has several advantages over other isolation techniques. The new method allows greater device density than does junction isolation in bulk silicon and maintains a functional advantage over silicon-on-sapphire by providing both MOS and bipolar capabilities.

2. Current Status of Work

The work on this project has been very successful. Although JSEP support was terminated on 31 August 1976, the research is continuing under new support provided by a contract from the Naval Electronics Laboratory Center. A paper entitled "Dielectrically Isolated Integrated Circuits Made with Preferential Etching" was accepted for presentation at the IEEE International Solid-State Circuits Conference on 18 February 1977; because this paper summarizes the high points of the work on this project, it is included as the final report.

DIELECTRICALLY ISOLATED INTEGRATED CIRCUITS MADE WITH PREFERENTIAL ETCHING

Phillip W. Barth, James B. Angell

A new dielectric isolation process based on chemical preferential etching of silicon has resulted in reproducible single-crystal layers less than $5 \mu\text{m}$ ($\pm 1 \mu\text{m}$) thick etched from a heavily doped starting wafer

with a lightly doped epilayer. The film is separated into islands by anisotropic etching and insulated by SiO_2 , Si_3N_4 , and polycrystalline silicon (poly-Si) to form such structures as the NPN transistor in Fig.

1. It has the following advantageous features:

- complete dielectric isolation, eliminating most parasitics
- an embedded conducting layer of poly-Si, which serves both as an additional layer of interconnection and as a lead to the underside of silicon islands
- device geometries smaller than those achievable with junction isolation
- self-alignment advantages similar to those of oxide-wall isolation schemes (such as LOCOS, ISOPLANAR)
- both MOS and bipolar capability for a functional advantage over SOS

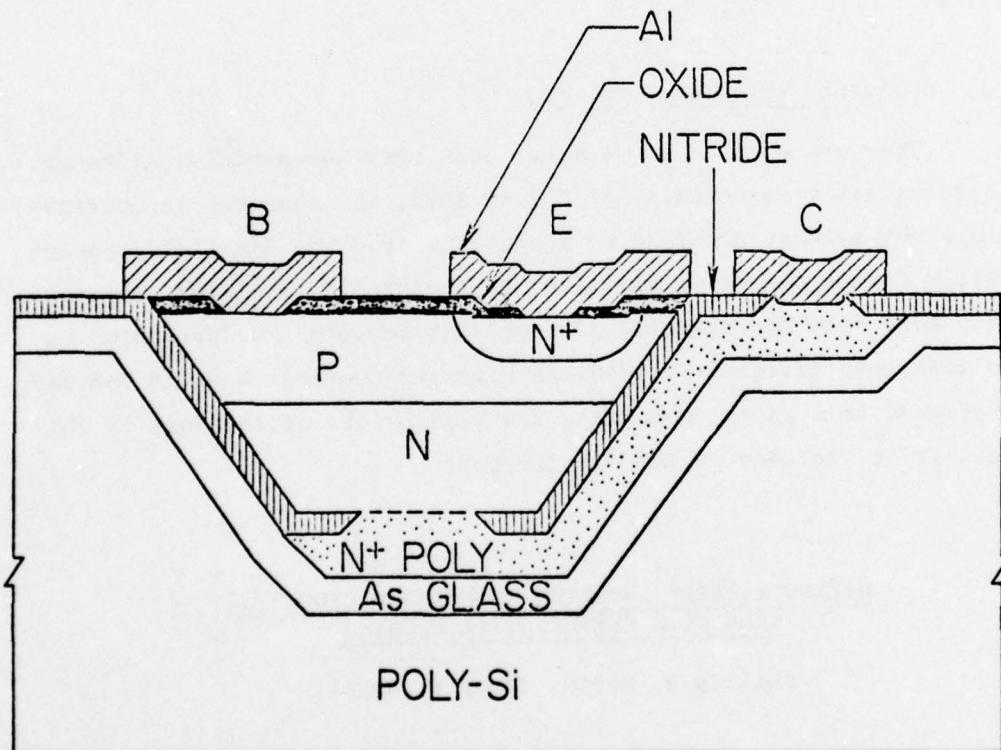


Fig. 1. DIELECTRICALLY ISOLATED NPN TRANSISTOR FORMED BY TRI-POLY PROCESS.

The steps in the dielectric isolation process, from the starting wafer to a final bipolar transistor structure, are described below with reference to Figs. 2, 3, and 4.

- (1) Figure 2: a 5 μm thick epitaxial layer is grown on a $\langle 100 \rangle$ oriented silicon wafer heavily doped with arsenic ($3 \times 10^{19}/\text{cm}^3$). A thermal oxide is grown on this epi-layer, and a layer of poly-Si approximately 200 μm thick is deposited as a "handle" for later processing.
- (2) The wafer is preferentially etched in a mixture of 1 HF: 3 HNO_3 :8 CH_3COOH , which removes the heavily doped starting substrate but stops etching at the lightly doped epilayer [1]. This etching step, unlike mechanical lapping, is tolerant of wafer warpage commonly encountered during deposition of the thick poly-Si layer [2], and its stopping point is more easily controlled than with mechanical lapping.

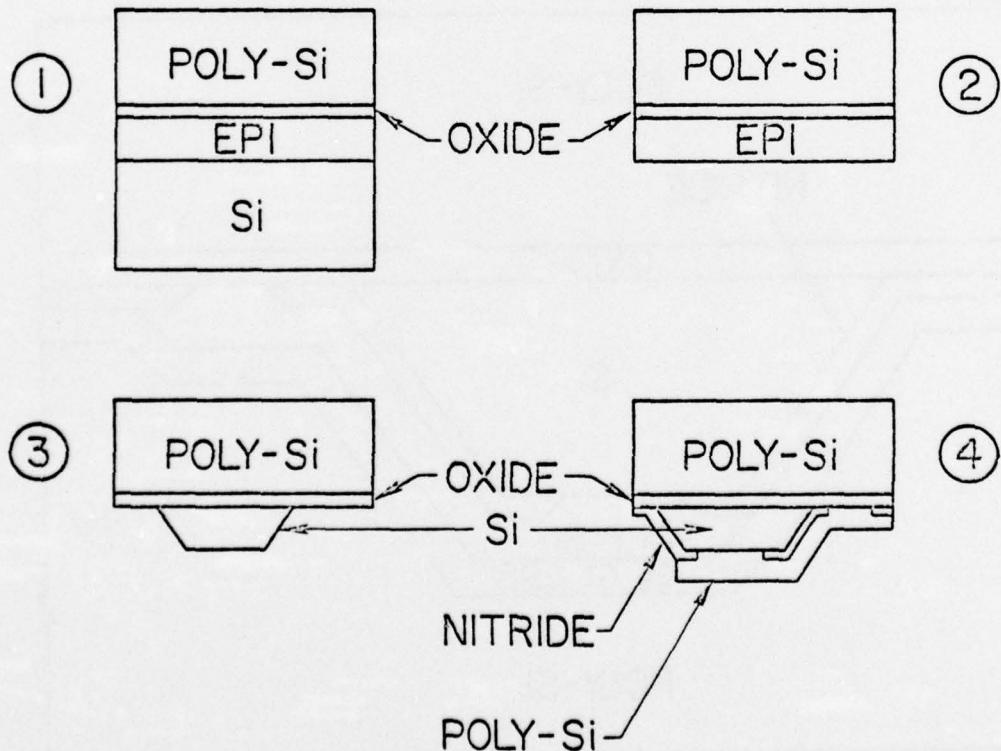


Fig. 2. STAGES IN TRI-POLY PROCESS.

- (3) A masked etch with KOH establishes islands of silicon which will later become active device regions.
- (4) A silicon-nitride layer is deposited over the surface; this layer will later act as both an insulator and an etch-stop region. Contact holes are defined in this layer, and a 1 μm thick poly-Si layer is deposited. A masking step defines a pattern in this thin poly-Si layer.
- (5) Figure 3: an oxide layer, heavily doped with arsenic, is deposited over the thin poly-Si layer, and then a thick (200 μm) layer of poly-Si is deposited as a supporting substrate for the end structure. During this deposition step, the As-doped oxide acts as a diffusion source to lower the resistivity of the 1 μm poly-Si layer.
- (6) Figure 4: the original 200 μm layer of poly-Si is etched away, exposing the original epitaxial surface. Three more masking steps (the base diffusion need not be a masked diffusion) suffice to form the bipolar transistor structure by standard predeposition and drive-in steps followed by contact holes and aluminum deposition and etching.

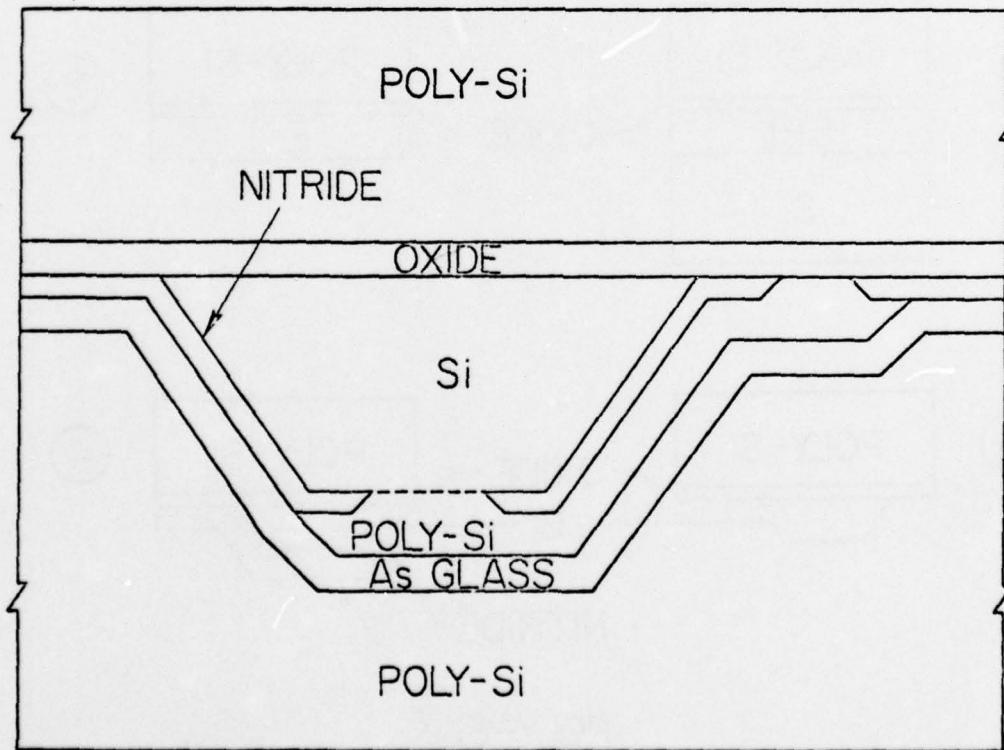


Fig. 3. THE TRI-POLY "SANDWICH" BEFORE REMOVAL OF TOP POLY-SI LAYER.

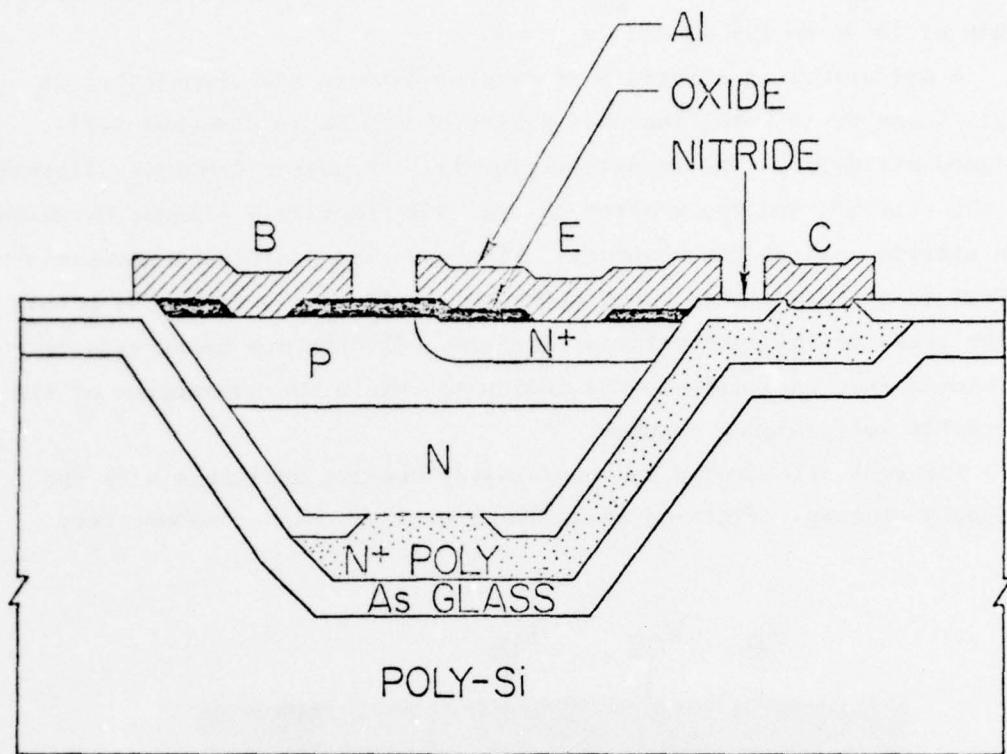


Fig. 4. TRI-POLY NPN TRANSISTOR WITH PARTIALLY SELF-ALIGNED EMITTER.

By returning to the original epitaxial surface, this tri-poly process (so called because of the three distinct poly-Si layers present in Fig. 3) avoids the pitted surface which is present after the preferential etching step. In addition, it produces a doping profile whose gradient is in the right direction (doping is light at the surface, heavier below).

Silicon nitride is used in this process to ensure good metal coverage. The buffered HF, used to etch oxide during masking steps, stops at the planar surface formed by Si, poly-Si, and nitride. This avoids a "trench" effect encountered during early runs at the Si-poly-Si boundary when only oxide was used as an insulator.

Preliminary work with the tri-poly process has produced vertical NPN and lateral PNP transistors which show good minority carrier lifetime and good carrier mobility in the dielectrically isolated silicon.

NPNs had $h_{fe} = 80$ with $BV_{CEO} = 22$ V, and lateral PNPs with a base-width of $10 \mu m$ on layout had $h_{fe} = 5$.

A difference in structure is evident between the transistors in Figs. 1 and 4; in both, the base diffusion can be an unmasked self-aligned diffusion. The transistor in Fig. 1 requires complete alignment of the emitter, and the emitter in Fig. 4 is partially aligned by using the nitride wall as one boundary. Figure 4 also contains a parasitic MOSFET (emitter = source, base = channel, collector = drain and gate) which leads to emitter-collector leakage. Efforts are being made to eliminate this parasitic MOSFET action to obtain the advantages of the partially self-aligned emitter.

Figure 5 illustrates the good layout density available with the tri-poly process. Pictured is an inverter stage of a complementary

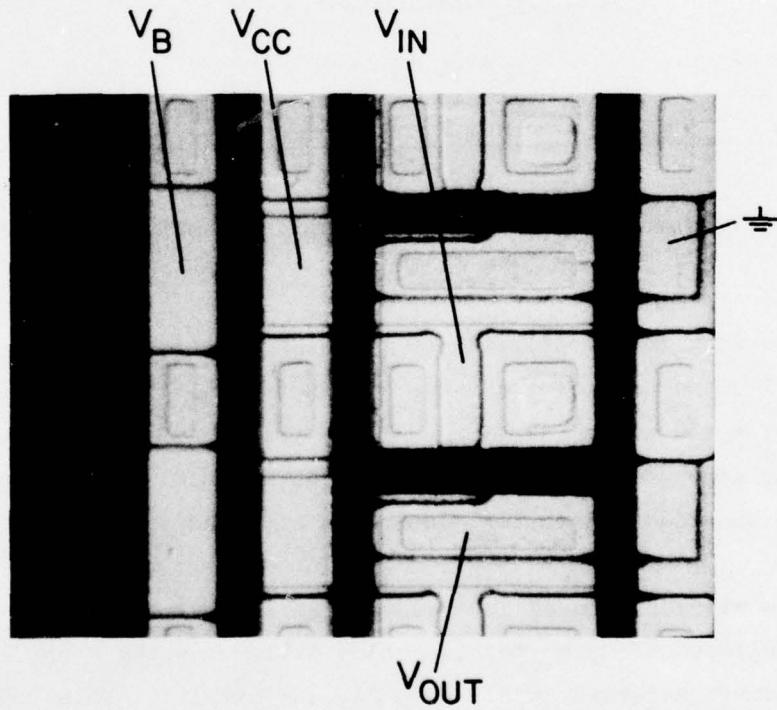


Fig. 5. SECTION OF COMPLEMENTARY TRANSISTOR LOGIC RING OSCILLATOR. Lateral PNP: base = V_B , emitter = V_{CC} , collector = V_{in} . Vertical NPN: base = V_{in} , emitter = ground, collector = V_{out} .

transistor logic ring oscillator, similar to an I^2L gate with the following variations on the I^2L structure: (a) the PNP base lead goes to a separate voltage line, (b) the NPN action is downward rather than upward, and (c) the NPN is Schottky clamped. This gate requires two extra aluminum lines (V_B and ground) as compared to an I^2L gate in bulk silicon, and extra space is taken up by the Schottky diode; however, the area is only 1.6 times that of an I^2L gate using the same layout rules. A straight reproduction of an I^2L inverter using the tri-poly process (including an extra line for ground) would have an area 0.6 times that of a bulk I^2L inverter.

References

1. H. Muraoka et al, "Controlled Preferential Etching Technology," Semiconductor Silicon 1973, Electrochem. Soc., p. 327.
2. T. I. Kamins, "Deformation Occurring during the Deposition of Polycrystalline Silicon Films," J. Electrochem. Soc., May 1974, p. 681.

B. Project 5012. IC PROCESS DESIGN AND COMPUTER MULTILAYER SEMICONDUCTOR DEVICE ANALYSIS

Principal Investigator: R. W. Dutton
Staff: D. B. Estreich

1. Objectives

Computer methods were developed to predict impurity profiles after processing, and physical parameters related to impurity diffusion were calculated.

Improved models will be developed for the prediction and simulation of multilayer semiconductor device behavior based on layout and device-processing history.

2. Current Status of Work

During this past reporting period, the following major accomplishments have been realized:

- improved parameter selection for a new user-oriented integrated injection logic (I^2L) macromodel that models current gain and injector transport efficiency falloff effects
- evaluation and design of second generation of special complementary MOS (CMOS) latch-up path test structures to allow separation of the relevant parameters associated with PNPN latch paths

The I^2L macromodel and CMOS latch-up work are a continuation of the research described in the last Status Report.

Previous work on modeling I^2L has been reported [1,2]; however, the models presented were applicable only to low-current operation. Recent emphasis has focused on modeling those aspects of I^2L that present severe limitations to I^2L performance and operational bounds [3,4]. This requires the modeling of both NPN current gain falloff resulting from base resistance (and emitter resistance in certain instances) and injector PNP current transport degradation at low- and high-current operating levels. Parameter measurement schemes have been developed and applied for base resistance and upward transit-time determination, including proper partitioning of multiple fan-out gates. With the inclusion of these effects in the macromodel, excellent agreement can be achieved between computer simulation and experimental results for all I^2L operating bias levels.

Recent work has also involved the study of latch-up mechanisms in CMOS integrated circuits and related merged structures. Two-dimensional analysis is required for adequately modeling latch-up action in integrated circuits. It has been demonstrated that accurate accounting for lateral spreading resistance is crucial in predicting latch-up conditions. In addition, field-aided lateral PNP current gain enhancement is being studied. New test structures have been designed to examine these factors.

References

1. D. B. Estreich, R. W. Dutton, and B. W. Wong, "An Integrated Injection Logic (I^2L) Macromodel Including Current Redistribution Effects," IEEE J. Solid-State Circuits, SC-11, Oct 1976, pp. 648-657.

2. D. B. Estreich and R. W. Dutton, "Modeling Integrated Injection Logic I^2L ," Tenth Annual Asilomar Conference on Circuits, Systems and Computers, Asilomar, Calif., 22 Nov 1976.
3. D. B. Estreich and R. W. Dutton, "Modeling Integrated Injection Logic (I^2L) Performance and Operational Limits," presented at International Solid-State Circuits Conf., Philadelphia, 16 Feb 1977.
4. D. B. Estreich and R. W. Dutton, "Modeling Integrated Injection Logic (I^2L) Performance and Operational Limits," submitted to IEEE J. of Solid-State Circuits for publication.

IV. SOLID STATE

A. Project 5111. TRANSPORT PROPERTIES OF $\text{Al}_x\text{Ga}_{1-x}\text{As}$, $\text{Al}_x\text{Ga}_{1-x}\text{Sb}$, AND $\text{In}_x\text{Ga}_{1-x}\text{As}$ SINGLE CRYSTALS

Principal Investigator: G. L. Pearson
Staff: K. Jew

1. Objective

The purpose of this project is a systematic study of the transport of free carriers in these ternary systems. The electronic parameters are free carrier mobility, resistivity, minority carrier diffusion length, activation energy, and trap energy levels. The distribution coefficients of selected doping impurities as a function of x are significant growth parameters. The results obtained should prove useful in the design of photoluminescent devices, injection lasers, solar cells, infrared detectors, and bulk-effect microwave devices.

2. Current Status of Work

Epitaxial layers of $\text{Al}_x\text{Ga}_{1-x}\text{As}$ were grown by liquid phase epitaxy techniques on [100] GaAs substrates. The melt solutions were prepared with 6N gallium, polycrystalline GaAs, and aluminum metal. Dopant impurities were Sn for n-type layers and Ge for p-type layers. To reduce unintentional impurities, the gallium melt was initially baked for more than 12 hours at 800°C in flowing high-purity hydrogen. After cooling to room temperature, substrates were inserted and source materials were added. Growth was carried out following saturation at 800°C through 1°C of supercooling before bringing the substrate into contact with the melt. The cooling rate was 0.2°C/min and growth terminated at 780°C.

During this investigation, two crystal-growth procedures have been used. In the first, the same melt was reused for several growth runs. Because the aluminum content in successive grown layers decreases as a result of depletion of Al from the melt, a range of ternary compositions can be obtained. In the second method, a fresh melt was prepared before each growth run. Most of the epitaxial layers were grown from reused melts. This method was discontinued, however, when it was found

that (1) precise growth data cannot be obtained because, in a series of growths, materials are depleted from the melt and the exact melt composition is unknown after the initial growth, and (2) the reused melts become contaminated as a result of oxidation of the Al during repeated cyclings of the system between room and growth temperatures, making it increasingly difficult to grow good quality crystals. Currently, $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers are grown from fresh melts only. These samples are expected to yield more reliable results for dopant and Al distribution coefficients and for electrical properties.

Photoluminescence measurements were made at 77° and 300°K on samples of (n) $\text{Al}_x\text{Ga}_{1-x}\text{As:Sn}$ with composition $0.0 \leq x \leq 0.50$. The band-gaps and alloy compositions were determined from the photoluminescence peak.

Electrical measurements of (n) $\text{Al}_x\text{Ga}_{1-x}\text{As:Sn}$ samples were made using Van der Pauw techniques. Ohmic contacts were formed by Au-Ge eutectic and alloying in hydrogen at 450°C. Carrier concentration, electron mobility, and resistivity were measured from 77° to 300°K. From the temperature dependence of the carrier concentration, the thermal activation energy of the Sn donor has been determined for $\text{Al}_x\text{Ga}_{1-x}\text{As}$ in the $0.0 \leq x \leq 0.50$ range. Results depend on the method used to grow the epitaxial layers. For (n) $\text{Al}_x\text{Ga}_{1-x}\text{As:Sn}$ crystals of similar compositions and carrier concentrations, the electron mobility of crystals grown from fresh melts is generally higher when compared to crystals grown from reused melts as a result of the decrease in crystalline quality.

Current study is directed toward LPE (p) $\text{Al}_x\text{Ga}_{1-x}\text{As:Ge}$ layers with compositions $0 \leq x \leq 1.0$. Van der Pauw, photoluminescence, and scanning electron microscope techniques are employed.

B. Project 5244. STUDIES OF HIGH-TRANSITION SUPERCONDUCTORS SUCH AS V₃Si AND Nb₃Sn AND DEPTH PROFILING OF Al_xGa_{1-x}As-GaAs HETEROJUNCTIONS

Principal Investigator: W. E. Spicer
Staff: I. Lindau, J. Miller, C. M. Garner

1. Objective

This project is involved in two separate areas of research. The first is to explore the electronic structures of type-II (hard) superconducting alloys, particularly the structure of Nb₃Sn, to determine such parameters as valence bandwidth which is important to the theoretical models of superconductors. Emphasis is directed toward the preparation of atomically clean Nb surfaces, followed by evaporation of Sn as an adlayer and annealing to form Nb₂Sn.

The second is to study the chemical interface between Al_xGa_{1-x}As and GaAs in this heterojunction system, particularly the chemical width of the junction and surface morphology of the interface for various aluminum concentrations ($0.3 \leq x \leq 0.85$). The Schottky barrier Au-Al_xGa_{1-x}As interface is also to be examined.

2. Current Status of Work

a. High-Transition Superconductors (I. Lindau, J. Miller)

Earlier work on a Nb single crystal indicated that the primary contaminants of the Nb surface were carbon, nitrogen, and oxygen. As a result, several Nb foils were purchased to investigate new methods for cleaning the samples. To determine the origin of the surface contamination, we elected to depth profile the carbon and oxygen signals. The Nb foils of better than 99.8 percent bulk purity were subjected to continuous cleaning by argon-ion sputtering. The Auger signals of oxygen and carbon were constantly monitored during the sputtering, and a clean surface was established with the carbon and oxygen signals falling below the noise level. The oxygen contamination reappeared immediately after sputtering, however, or when the argon beam energy was reduced below 500 eV.

Measurements of the partial pressure of O₂ and CO with a mass spectrometer indicated that all of the contamination could not stem

from the background gases present in the chamber. One mechanism proposed to explain the almost immediate reappearance of the contaminants was diffusion from the bulk.

In other work, successful removal of carbon was accomplished by heating the sample to 1700°C for three hours. Light sputtering removed the nitrogen, but most of the oxygen signal remained.

b. Depth Profiling (C. M. Garner)

Auger profiles have been made on $\text{Al}_x\text{Ga}_{1-x}\text{As}$ -GaAs heterojunctions [grown by abrupt liquid phase epitaxy (LPE) techniques] for $x = 0.3, 0.43, 0.60$, and 0.85 . The interface width (90 to 10 percent Al Auger signal) was found to be $\sim 100 \text{ \AA}$ for samples grown at 750°C and 130 \AA for samples grown at 800°C . The growth mechanisms and dependence of the interface width on growth temperature and time are being investigated.

Additional studies have included the InGaAsP-InP interface of samples grown by LPE and VPE. The LPE samples were found to behave as predicted by the growth conditions; however, the VPE InP layer displayed an unusual composition with depth (it appeared that the Ga had diffused out of the InGaAsP layer into the InP). Further work will be directed toward understanding this effect.

Auger profiles of the Au- $\text{Al}_x\text{Ga}_{1-x}\text{As}$ interface revealed the presence of an oxide layer in samples that had been etched prior to being placed in the Au evaporation chamber; this layer is approximately the same thickness as the native oxide layer. Current work is directed at removing the oxide layer and evaporating Au in situ to avoid the formation of an oxide layer. The electrical properties of these contacts will then be studied to understand the effect of the oxide.

V. RADIOSCIENCE

A. Project 3172. DIGITAL IMAGE PROCESSING

Principal Investigator: R. N. Bracewell
Staff: J. Mandeville

1. Objective

The purpose of this project is to evaluate and improve algorithms for digital image processing with a priori information.

2. Current Status of Work

This project will become active on 1 January 1977.

B. Project 3476. DEVELOPMENT OF AN AUDIO-TRACKING FILTER/ANALYZER

Principal Investigator: R. A. Helliwell
Staff: E. Paschal

1. Objective

Variable frequency narrowband VLF signals in the magnetosphere are difficult to analyze. At present, we record VLF signals at field stations and process the recordings at Stanford, using a spectrum analyzer to generate photographic spectral records. It is difficult, however, to determine the amplitude of individual signals in the filmed spectra. One solution is to use a frequency-tracking filter that can follow the changing frequency of an individual signal and separate it from other signals present in the tape-recorded data so that its amplitude as a function of time can be measured. The purpose of this project is to develop such a filter, capable of tracking signals over the range from 50 Hz to 30 kHz. The filter will have selectable bandwidths from 10 Hz to 1 kHz wide and will be capable of tracking signals that change frequency at rates up to 20 kHz/sec.

2. Current Status of Work

The design of the system is approximately 90 percent complete, and the construction is 70 percent finished. We estimate that another two man-months will be required to complete the project. Because the project leader (E. Paschal) will be working in the Antarctic from October 1976 until March 1977, the project should be finished sometime in May 1977.

The tracking filter uses a local oscillator and mixer to translate the input-signal spectrum into the passband of an IF filter with a center frequency of 100 kHz. The output of the filter is then fed to a frequency discriminator whose output controls the LO frequency to cause the system to follow the input-signal component as it changes frequency. The tracking filter system can be divided into two parts--the IF filter and discriminator assembly and the local oscillator and track-control assembly.

a. IF Filter and Discriminator Assembly

The IF filter uses conventional analog techniques to filter the input signal; actually, several filter elements are used in series. The input signal at 100 kHz is run through a three-pole Butterworth filter with a bandwidth of 3 kHz and is then mixed with a 70 kHz tone. The 30 kHz difference spectrum is then filtered with another three-pole filter with a 1 kHz bandwidth, and the output is translated down to 10 kHz. This process is repeated with successive filters with bandwidths of 300, 100, and 30 Hz and finally with a 10 Hz bandwidth filter centered at 300 Hz. System bandwidths of 10, 30, 100, 300 Hz, and 1 kHz are obtained by selecting the output of the appropriate filter. Each filter has a matching discriminator, and the output of the selected discriminator is used to control the local oscillator. The IF filters and discriminators employ temperature-compensated L-C resonators.

This multiple-conversion approach makes it possible to build a variable bandwidth filter with a given (input) frequency without resorting to crystal resonators which would be required if all the filtering were to be done at 100 kHz. The spurious response to out-of-band signals should also be less than with a crystal filter. The IF filter and discriminator assembly are nearly one-half completed.

b. Local Oscillator and Track Control

This part of the system uses all digital circuits and has been the most interesting segment of the design. To track a signal, the local oscillator is set to such a frequency that the signal, when it appears, will be translated into the passband of the IF filter. The LO frequency runs from 100 to 130 kHz. It is necessary to set the initial frequency of the LO with sufficient accuracy so that the translated signal is within the passband of the IF filter; with a filter bandwidth of 10 Hz, this means that the oscillator must be set within ± 5 Hz of the correct frequency. Because such accuracy at a frequency of 100 kHz was deemed beyond the ability of an analog oscillator, a digital frequency synthesizer has been designed for the LO.

The synthesizer uses a novel form of direct digital synthesis. Its output is a square wave at a frequency from 100 to 130 kHz. The jitter in the square wave is approximately 3 nsec rms and, as a result, spurious synthesizer signals are at least 60 dB below the fundamental. (A spurious LO signal appears in the system as a spurious filter response and must be kept as small as possible.) The synthesizer can be controlled in 1 Hz steps and has an accuracy of 0.1 Hz. CMOS logic is used, and the synthesizer consumes approximately 5 W of power. Its design is apparently new and may be patented.

Using a digital frequency synthesizer for the local oscillator also simplifies the frequency and tracking-control circuits. The initial frequency-set and the frequency and slew-rate-limit circuits are all digital. The construction of the local oscillator and track-control circuits is approximately 95 percent complete.

C. Projects 3606 and 4504. MEASUREMENTS OF METEOROLOGICAL PARAMETERS
IN THE LOWER TROPOSPHERE

Principal Investigators: A. M. Peterson, V. R. Eshleman,
A. T. Waterman, Jr., M. Frankel
Staff: N. Bhatnagar, S. J. Wernecke, R. W. Lee, R. D.
Fleming

1. Objective

The objective of this research is the investigation of atmospheric parameters and phenomena in the lower troposphere based on two

different but complementary techniques--radio acoustic sounding (RASS) and radio propagation in the S- and K-bands. The goals of each method are as follows.

a. RASS (Project 3606)

- Measuring real-time vertical temperature and horizontal wind profiles over a 1 km (or greater) range, using both RASS and conventional techniques.
- Obtaining temperature and horizontal wind profiles over extended periods of time and through varying meteorological conditions.
- Monitoring atmospheric phenomena continuously (with sampling periods of less than 5 minutes).
- Studying the interaction of electromagnetic and acoustic waves in a stochastic atmosphere characterized by turbulence, mean winds, and temperature gradients.

b. Tropospheric Radio Propagation (Project 4504)

- Measurement of wind velocity in the common volume of a transhorizon troposcatter propagation path by means of doppler techniques.
- Probing the structure of winds and turbulence in the lower troposphere under various conditions of atmospheric stability and instability.

2. Current Status of Work

a. RASS (Project 3606)

In the Stanford Radio Acoustic Sounding System (RASS), an electromagnetic signal is made to scatter from a moving acoustic pulse train. Under a Bragg-scatter condition, maximum electromagnetic scattering occurs. The scattered radio signal contains the signature of the atmosphere as a function of the acoustic-pulse position.

In the analysis of the RASS to date, such atmospheric conditions as turbulence, humidity, mean temperature, and mean wind fields have been ignored. In this study, system performance is assessed

in a real atmosphere. The only assumption made is that the acoustic wave train (not the EM wave) is affected by stochastic perturbations in the atmosphere.

Coherency of vertical acoustic-wave propagation is described through a perturbation-theoretic method and Feynman's diagrammatic technique. One of the most important attributes of this analysis is that it systematically and explicitly accounts for multiple scattering of acoustic waves in the presence of atmospheric fluctuations. The coherency results are then applied to evaluate the strength of the scattered electromagnetic signal from the acoustic pulse train, while taking into account the presence of turbulence, mean temperature, and mean wind fields.

From this study, we conclude that, for acoustic pulses with carrier frequencies below a few kilohertz propagating under typical atmospheric conditions, turbulence has little effect on the strength of the received radio signal at heights up to a few kilometers. This result implies that focusing of RF energy by the acoustic wavefronts is primarily a function of sound intensity which decreases as x^{-2} , where x is the altitude.

The effect of mean vertical wind and mean temperature on the strength of the received signal is also shown to be insignificant. Mean horizontal winds, however, shift the focus of the reflected electromagnetic energy from its origin, resulting in a decrease in received signal level when a monostatic RF system is used. In a bistatic radar configuration with space-diversified receiving antennas, the shifting of the acoustic pulse makes possible the remote measurement of the horizontal wind component.

These theoretical analyses have been supported experimentally. A high-frequency RASS operating at an acoustic frequency of 1 kHz and a radio frequency of 440 MHz was constructed at the Stanford Research Institute. Consistent with theoretical predictions, this system was able to provide both doppler data and horizontal wind profiles over a range of 1 km.

These experimental results came from a brief endeavor to support our theoretical studies. Future experiments could extend the

profiling range and versatility of the high-frequency RASS; it could become a valuable tool for the remote real-time measurement of atmospheric temperature, winds, and wind-shear. Through further research, we hope to provide a mobile system capable of producing these data at any location desired by a user.

During the next reporting period, we intend to complete our theoretical research and submit it for publication.

b. Tropospheric Radio Propagation (Project 4504)

As outlined in the last status report, the wind-measuring technique is to involve the simultaneous reception of 3-GHz CW signals on each of two narrow beams from a transmitter located 100 miles away (beyond line-of-sight). The two beams are aimed on either side of the great-circle bearing toward the transmitter by small amounts (1° or less). If there is a wind component transverse to the path in the region of the common volume, it is anticipated that the signal received on one beam will be doppler shifted to higher frequencies and the signal on the other to lower frequencies. The magnitude of the doppler difference should be proportional to transverse-wind velocity. The two beams will be formed during the data-reduction procedures because the receiving antenna is a sampling array that measures and stores on digital tape the amplitudes and phases of the signal as received on 12 individual antennas. To obtain high resolution in azimuth, the antennas are arranged in a horizontal linear array.

The linear array to be used for this purpose is a series of 12 4-ft parabolic dishes mounted on a 70-ft tower. The tower had been used in previous experiments in a vertical position. For the current work, it was necessary to move the tower to a horizontal position, and this move has been accomplished. The balance of the equipment has been checked and is in operating condition; however, the measurement program has been delayed because one of the key personnel is on leave of absence.

In the meantime, some work has been directed toward the second of the two objectives, involving line-of-sight rather than trans-horizon paths.

D. Project 4214. INVESTIGATION OF UNDERSEA COMMUNICATION WITH ULF ELECTROMAGNETIC WAVES

Principal Investigator: O. G. Villard, Jr.
Staff: A. C. Fraser-Smith, D. M. Bubenik, A. Ho

1. Objective

The feasibility of using ULF electromagnetic waves (frequencies of less than 5 Hz) from electric and magnetic dipole sources will be investigated for undersea/undersea communication in the approximate range of 0 to 20 km.

2. Current Status of Work

This is a new project; work commenced in September 1976. The theoretical expressions for the ULF electric and magnetic fields produced in sea water by submerged vertically directed magnetic and electric dipoles (with a sea floor present) have been programmed for numerical solution. Numerical solution is in progress, and exact data concerning ULF fields will become available shortly. We will then be in a position to evaluate the feasibility of using these fields for communication beneath the sea.

VI. PLASMA PHYSICS AND QUANTUM ELECTRONICS

A. Project 1328. VERY LONG DELAYED RADIO ECHOES

Principal Investigator: F. W. Crawford
Staff: R. J. Vidmar, T. L. Savarino

1. Objective

There is evidence indicating that radio signals can occasionally be returned from the ionosphere with delays of the order of tens of seconds, rather than the few milliseconds corresponding to direct reflection. The objective of this project is to develop a theoretical explanation of this phenomenon.

2. Current Status of Work

Earlier theoretical studies [1] have suggested the following plausible mechanism for long-delayed echoes. When an ordinary wave from the transmitter reaches its reflection point, near the peak of the F-layer, it is partially converted into a longitudinal plasma wave. This wave is amplified by energetic electrons precipitating down Earth's magnetic field lines and propagates with very low group velocity ($\approx 1 \text{ km/sec}$) over a distance of several kilometers. The longitudinal plasma wave is partially converted into a transverse electromagnetic wave as it propagates down the ionospheric electron-density gradient, and this wave propagates to the receiver.

Work was performed on this project only during the first two months of the reporting period. Effective 1 September 1976, the project was transferred to other sponsorship. The work performed before termination was directed toward an understanding of the process by which the amplified longitudinal plasma wave is coupled to a transverse electromagnetic wave which can propagate out of the ionosphere. Specifically, the coupling into an ordinary wave has been studied in the region $\omega \approx \omega_p$, near the ordinary wave reflection point. Coupling between these wave modes is assumed to occur as a result of Earth's magnetic field and an inhomogeneity in the ambient electron density. Even with a simple model of this amplified longitudinal wave, significant coupling into the

ordinary wave is predicted, confirming preliminary estimates made in the last reporting period. The more complicated step, to develop a model of the mechanism that couples energy into longitudinal waves from the electromagnetic waves produced by the ground transmitter, is being pursued under NSF sponsorship.

Reference

1. D. M. Sears, "Long Delayed Echoes," Stanford University Institute for Plasma Research Report No. 584, Stanford University, Stanford, Calif., Nov 1974.

B. Hansen Laboratories. TWO-PHOTON RESONANTLY PUMPED IR UP-CONVERTERS

Principal Investigators: S. E. Harris, J. F. Young
Staff: J. H. Newton

1. Objective

The goals of this project are the development and extension of efficient IR up-conversion techniques in metal vapors, particularly image up-conversion.

2. Current Status of Work

During the previous reporting period, we demonstrated the up-conversion of $2.9 \mu\text{m}$ IR images to 4550 \AA in Cs vapor. A power efficiency of 20 percent with over 1000 resolvable spots was achieved using a pump power of only 8 kW focused in an area of 0.1 cm^2 . The Cs cell had an active length of 0.2 cm and was operated at a density of $1.4 \times 10^{17}/\text{cc.}$ The pumping laser, Nd:lanthanum berylate, has a natural two-photon coincidence with the Cs $6s^2S-7s^2S$ transition, resulting in a simple practical system with a number of potential applications.

We have since designed and constructed a new Cs IR imaging system that should have significantly increased resolution and efficiency. As seen in Table 1, this increase will be accomplished through higher number density Cs cells of larger area. For comparison, Table 1 also lists the parameters for a LiNbO_3 up-converter having the same performance; the crystal system requires 1250 times more pump power.

Table 1

DESIGN PARAMETERS FOR A Cs AND LiNbO₃ 2.9 μ UP-CONVERTER

Parameter	Cs	LiNbO ₃
Pump wavelength (μ)	1.0790	1.06
IR wavelength (μ)	2.94	2.94
Sum wavelength (\AA)	4560	7800
Pump bandwidth (cm^{-1})	0.1	≈ 1.0
Pump pulselength (nsec)	50	50
Photon efficiency (%)	27.5	27.5
Resolution	10^5	10^5
Pump power (W)	1.44×10^5	9×10^7
Cs density (cm^{-3})	4.44×10^{17}	---
Area (cm^2)	3.74	2
Length (cm)	0.2	0.46

As a result of attacks by the Cs vapor, our earlier cells have had short lifetimes (approximately 24 hours). The new design incorporates features that should make it more impervious to attack and substantially increase the lifetime.

The cell used in the demonstration of the IR up-conversion consisted of two metalized sapphire windows brazed to kovar rings. The rings were heliarced to Varian conflat flanges that were then bolted together by means of standard copper gaskets. A nickel side arm was heliarced to the flanges. The spacing between the windows was 0.2 cm. The apparent failure of the cell occurred at the braze between the sapphire and kovar ring. As a result, we have decided on a radically different cell design (see Fig. 6) consisting of two 2-inch in diameter sapphire windows pressed against an optically polished stainless-steel plate 0.2 cm thick. In the center of the plate will be a hole 1.25-inch in diameter to produce a 3/8-inch seal around each window. Each sapphire window will be pressed

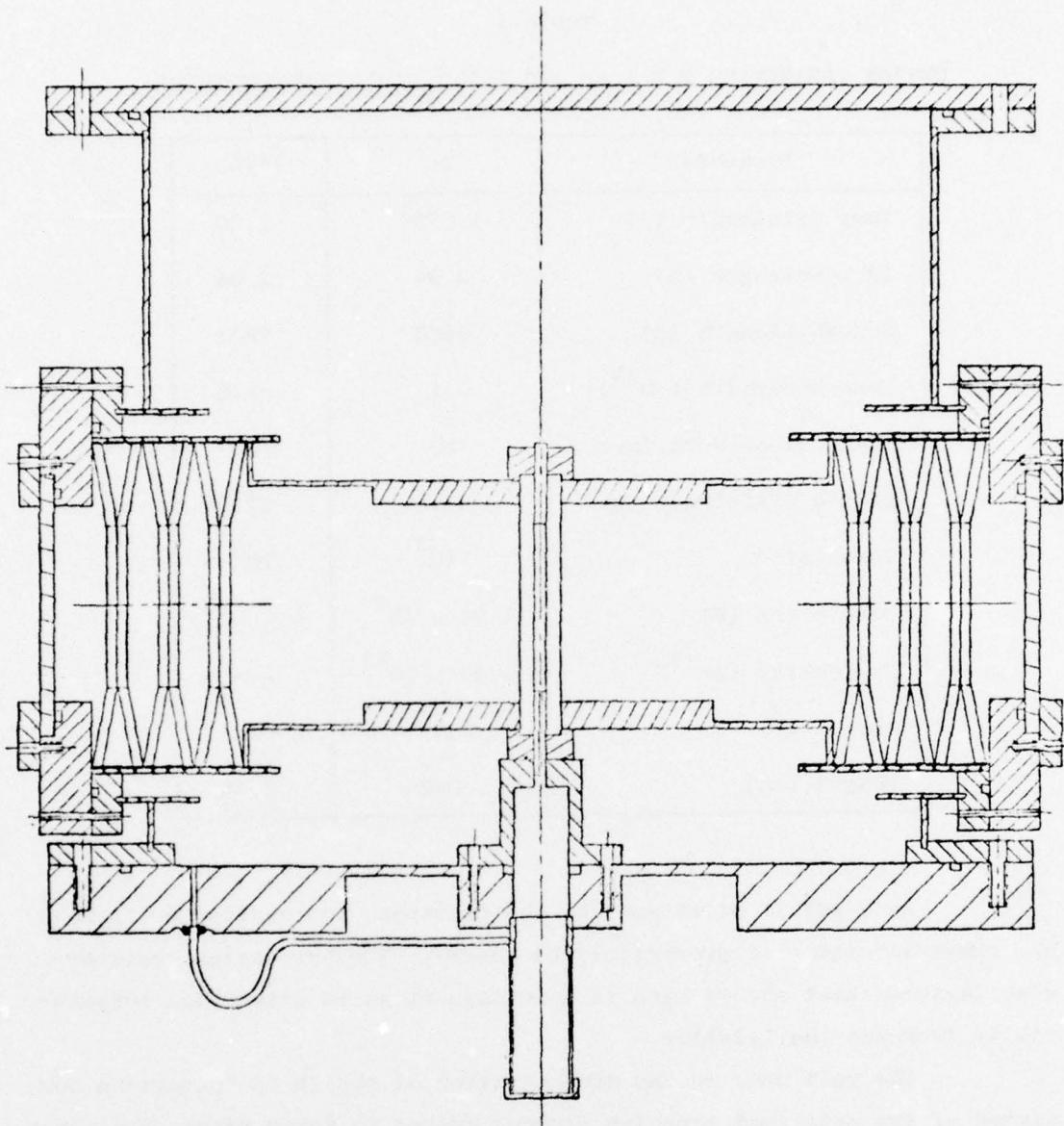


Fig. 6. NEW Cs CELL DESIGN.

against the polished plate by means of an annulus spring loaded by a stack of Belleville spring washers held by the port window flanges of the cylindrical outer cell. Two-inch infrasil quartz windows will be rubber o-ring sealed to the port window flanges. The stainless-steel plate will be electron-beam welded to a hollow cylindrical stainless-steel support, and the

support will be metal o-ring sealed to the base plate. The base plate has a thin-walled stainless-steel side arm heliarced to it. A 0.1 cm hole connects the hole in the center of the polished stainless plate and the side arm, and a capillary tube connects the side arm to a hole in the base plate. To load the cell, a clean glass ampoule of Cs is inserted in the side arm. Evacuating the outer cell evacuates the space between the sapphire windows and the side arm via the capillary tube. The ampoule is then crushed by flexing the thin-walled side arm. When the side arm is heated, Cs will begin to leak out through the tube but will condense at the end farthest from the side arm and clog the tube. The only escape route for the Cs will be by diffusion across the 3/8-inch seal between the sapphire windows and the polished plate, which hopefully will be quite slow. Thermocouple and heater connections to the inner cell will be made by vacuum feedthroughs in the base plate. Construction of the new cell is approaching completion; the only remaining work is the polishing and electron-beam welding of the stainless-steel plate.

We recently learned of two different methods for contacting sapphire to niobium--active brazes such as nickel-niobium and titanium-vanadium alloys and calcium aluminate frit. Both the frit and the brazes are extremely resistant to attack by Cs vapor. Because niobium is not attacked by Cs and its coefficient of thermal expansion is compatible with sapphire, construction of an all-niobium cell with sapphire windows is possible. If the lifetime of this cell design proves to be inadequate, we shall pursue the development of a niobium-sapphire cell that could be mounted in the outer cell. Evacuation of the outer cell would be required because niobium is susceptible to severe oxidation at elevated temperatures.

Long-lifetime cells are particularly important because a major goal will be to make a careful measurement and characterization of image quality. The image resolution, contrast, coma, and other aberrations will be measured and compared to theory; methods of correction where necessary will be examined.

Appendix A

OUTSIDE PUBLICATIONS

1. Papers Presented at Meetings

Information Systems

Cover, T. and J. van Campenhout, "On the Possible Orderings in the Measurement Selection Problem," Third International Joint Conf. on Pattern Recognition, Coronado, Calif., 8-11 Nov 1976.

Cover, T., "Descriptive Structure of Pattern Recognition," Third International Conf. on Pattern Recognition, Coronado, Calif., 8-11 Nov 1976.

Friedlander, B., M. Morf, T. Kailath, and L. Ljung, "Levinson- and Chandrasekhar-Type Equations for a General Discrete-Time Linear Estimation Problem," 1976 Decision and Control Conf., Fla., Dec 1976.

Gill, J. and I. Simon, "Ink, Dirty-Tape Turing Machines, and Quasi-complexity Measures," Third International Colloquium on Automata, Languages, and Programming, Edinburgh, Scotland, Jul 1976.

Hellman, M., "Low Cost Data Compression," International Telemetering Conf., Los Angeles, 28-30 Sep 1976.

Kailath, T., L. Ljung, and M. Morf, "Recursive Input-Output and State-Space Solutions for Continuous-Time Linear Estimation Problems," 1976 Decision and Control Conf., Fla., Dec 1976.

Kung, S-Y., T. Kailath, and M. Morf, "A Generalized Resultant Matrix for Polynomial Matrices," 1976 Decision and Control Conf., Fla., Dec 1976.

Ljung, L. and T. Kailath, "Formulas for Efficient Change of Initial Conditions in Linear Least Squares Estimation," 1976 Decision and Control Conf., Fla., Dec 1976.

Macovski, A. and D. Rosenfeld, "Source Dependent Imaging in Nuclear Medicine," IEEE Symposium on Computer-Aided Diagnosis of Medical Images, Coronado, Calif., 11 Nov 1976.

Morf, M., L. Ljung, and T. Kailath, "Fast Algorithms for Recursive Identification," 1976 Decision and Control Conf., Fla., Dec 1976.

Rosenfeld, D. and A. Macovski, "A New Method for Three-Dimensional Imaging in Nuclear Medicine," Annual Conf. on Engineering in Medicine and Biology, Boston, Mass., 8 Nov 1976.

Digital Systems

Owicki, S. S., "Verifying Monitors," IFIP Working Group 2.2, Tampere, Finland, 23-27 Aug 1976.

Terman, F. W., "A Study of Interleaved Memory Systems by Trace Driven Simulation," Fourth Symposium on the Simulation of Computer Systems, Boulder, Colo., 10 Aug 1976.

Integrated Circuits

Barth, P. W. and J. B. Angell, "Dielectrically Isolated Integrated Circuits Made with Preferential Etching," IEEE International Solid-State Circuits Conf., 18 Feb 1977.

Estreich, D. B. and R. W. Dutton, "Modeling Integrated Injection Logic (I^2L)," Tenth Annual Asilomar Conf. on Circuits, Systems, and Computers, Asilomar, Calif., 22 Nov 1976.

Estreich, D. B. and R. W. Dutton, "Modeling Integrated Injection Logic (I^2L), Performance and Operational Limits," International Solid-State Circuits Conf., Philadelphia, 16 Feb 1977.

Solid State

Garner, C. M., Y. D. Shen, G. L. Pearson, and W. E. Spicer, "Auger Profiling of Interface Widths of $Al_xGa_{1-x}As$ Heterojunctions," meeting of the Am. Phys. Soc., Stanford University, Stanford, Calif., 20-22 Dec 1976. Abstract published in Bull. Am. Phys. Soc., 21, 1976, p. 1290.

Garner, C. M., Y. D. Shen, G. L. Pearson, and W. E. Spicer, "Auger Profiling of Interface Widths of $Al_xGa_{1-x}As$ Heterojunctions Grown by LPE," meeting of the Am. Phys. Soc., Stanford University, Stanford, Calif., 20-22 Dec 1976.

Houng, Y. M., B. L. Mattes, and G. L. Pearson, "Deep Trapping Effects at the GaAs-GaAs:Cr Interface in GaAs FET Structures," meeting of the Am. Phys. Soc., Stanford University, Stanford, Calif., 20-22 Dec 1976.

Mattes, B. L., Y. M. Houng, and G. L. Pearson, "Growth and Properties of Semi-Insulating LPE GaAs for FET Buffer Layers," meeting of the Am. Phys. Soc., Stanford University, Stanford, Calif., 20-22 Dec 1976.

Shen, Y. D., C. M. Garner, W. E. Spicer, and G. L. Pearson, "Growth and Analysis of Thin LPE n-($Al_{0.44}Ga_{0.56}As$) Layers on n-GaAs," meeting of the Am. Phys. Soc., Stanford University, Stanford, Calif., 20-22 Dec 1976. Abstract published in Bull. Am. Phys. Soc., 21, 1976, p. 1290.

Radioscience

Frankel, M. S., "A High-Frequency Radio Acoustic Sounder for Remote Measurement of Atmospheric Winds and Temperature," Atmospheric Acoustics Workshop, Acoustical Society of America, San Diego, 18 Nov 1976.

2. Papers Published

Information Systems

Cover, T., "Open Problems in Information Theory," Proc. of 1975 USSR Joint Workshop on Information Theory, IEEE Press, 1976, pp. 35-36.

Cover, T. and T. Wagner, "Topics in Statistical Pattern Recognition," chapter in Digital Pattern Recognition (Communication and Cybernetics, Vol. 10; Fu, Keidel, and Wolter, eds.), Springer-Verlag, 1976, pp. 15-46.

Fine, T. and J. Gill, "The Enumeration of Comparative Probability Relations," Annals of Probability, 4, Aug 1976, pp. 667-673.

Gray, J. and D. S. Ornstein, "Sliding-Block Joint Source/Noisy-Channel Theorems," IEEE Trans. on Information Theory, IT-22, Nov 1976, pp. 682-690.

Kailath, T. and L. Ljung, "Asymptotic Behavior of Constant-Coefficients Riccati Differential Equations," IEEE Trans. on Automatic Control, AC-21, 3, Jun 1976, pp. 385-388.

Ljung, L. and T. Kailath, "Backwards Markovian Models for Second-Order Stochastic Processes," IEEE Trans. on Information Theory, IT-22, 4, Jul 1976, pp. 488-491.

Weinert, H. L. and T. Kailath, "A Spline-Theoretic Approach to Minimum-Energy Control," IEEE Trans. on Automatic Control, AC-21, 3, Jun 1976, pp. 391-393.

Digital Systems

Lee, R. B., "Performance Bounds for Parallel Processors," TR No. 125, Stanford Electronics Laboratories, Stanford University, Stanford, Calif., Nov 1976.

Losq, J., "Effects of Failures on Performance of Gracefully Degradable Systems," Tech. Note No. 103, Digital Systems Laboratory, Stanford University, Stanford, Calif., Dec 1976.

Losq, J., "Efficiency of Compact Testing for Sequential Circuits," Tech. Note No. 104, Digital Systems Laboratory, Stanford University, Stanford, Calif., Dec 1976.

Terman, F. W., "A Study of Interleaved Memory Systems by Trace Driven Simulation," Tech. Note No. 94, Digital Systems Laboratory, Stanford University, Stanford, Calif., Sep 1976.

Integrated Circuits

Estreich, D. B., R. W. Dutton, and B. W. Wong, "An Integrated Injection Logic (I^2L) Macromodel Including Current Redistribution Effects," IEEE J. Solid-State Circuits, SC-11, Oct 1976, pp. 648-657.

Plasma Physics and Quantum Electronics

Stappaerts, E. A., S. E. Harris, and J. F. Young, "Efficient IR Image Up-Conversion in Two-Photon Resonantly Pumped Cs Vapor," Appl. Phys. Lett., 29, Nov 1976, p. 669.

3. Papers Accepted for Publication

Information Systems

Carleial, A. B. and M. E. Hellman, "A Note on Wyner's Wiretap Channel," IEEE Trans. on Information Theory, May 1977.

Cover, T., "Comments on Stone's Paper," Annals of Statistics, 1977.

Cover, T. and A. Shenhav, "Compound Bayes Predictors for Sequences with Apparent Markov Structure," IEEE Trans. on Systems, Man, and Cybernetics, Jun 1977.

Cover, T. and C. Keilers, "An Offensive Statistic for Baseball," JORSA, 1977.

Gill, J., "Computational Complexity of Probabilistic Turing Machines," SIAM J. on Computing.

Gray, R. and M. B. Pursley, "A Source Coding Theorem for Stationary Measurable Continuous Time Random Processes," Annals of Probability.

Kailath, T., L. Ljung, and M. Morf, "Generalized Krein-Levinson Equations for Efficient Calculation of Fredholm Resolvents of Non-displacement Kernels," Advances in Mathematics, 1977.

Kung, S., T. Kailath, and M. Morf, "Fast and Stable Algorithms for the Minimal Design Problems," IFAC, 1977.

Ljung, L. and T. Kailath, "Efficient Change of Initial Conditions, Dual Chandrasekhar Equations and Some Applications," IEEE Trans. on Automatic Control, 1977.

Morf, M., A. Vieira, and T. Kailath, "The Multichannel Maximum Entropy Method," J. Geophys., 1977.

Morf, M., L. Ljung, and T. Kailath, "Fast Algorithms for Recursive Identification," IEEE Trans. on Automatic Control, 1977.

Morf, M., B. Levy, S-Y. Kung, and T. Kailath, "New Results on the 2D Systems Theory," IEEE Trans. on Automatic Control, special issue on Multidimensional Systems, 1977.

Morf, M. and T. Kailath, "Recent Results in Least-Squares Estimation Theory," Annals of Economic and Social Measurement, 1977.

Morf, M., B. Levy, and S-Y. Kung, "New Results on 2-D Systems Theory," Part I: "2-D Polynomial Matrices, Factorization, and Coprimeness," Proc. IEEE, 1977.

Morf, M., B. Levy, S-Y. Kung, and T. Kailath, "New Results on 2-D Systems Theory," Part II: "2-D State-Space Models--Realization and the Notions of Controllability, Observability, and Minimality," Proc. IEEE, 1977.

Vieira, A. and T. Kailath, "On Another Approach to the Schur-Cohn Criterion," IEEE Trans. on Circuits and Systems, 1977.

Integrated Circuits

Estreich, D. B. and R. W. Dutton, "Modeling Integrated Injection Logic (I^2L) Performance and Operational Limits," IEEE J. Solid-State Circuits.

Solid State

Cheng, K. Y. and G. L. Pearson, "The Al-Ga-Sb Ternary Phase Diagram and Its Application to Liquid Phase Epitaxial Growth," J. of Electrochem. Soc..

Appendix B

ABSTRACTS OF REPORTS PUBLISHED DURING THIS PERIOD

**This appendix is a compilation of abstracts of reports issued by
the Stanford Electronics Laboratories (SEL).**

A STUDY OF INTERLEAVED
MEMORY SYSTEMS BY
TRACE DRIVEN SIMULATION
by Fred W. Terman

JSEP Contract
N00014-75-C-0601
Tech. Note No. 94
September 1976

ABSTRACT

A model of interleaved memory systems for IBM 360/370 architecture has been investigated by means of a trace driven simulation. The model used is an extension of one due to G. J. Burnett and E. G. Coffman, Jr. The trace data to drive the simulation was obtained from traces of typical IBM 360/370 programs and of the OS/VS2 operating system. The predictions of the Burnett-Coffman model are found to fit well with the simulation results for the fetching of instructions. For the fetching of operands, however, the simulation results show only about half the increase in the memory bandwidth that the Burnett-Coffman analysis predicts. This indicates that data references on the IBM 360/370 are not random in the way assumed by Burnett and Coffman.

ABSTRACT

New propagation models have been developed for the study of the ducting of whistlers. Two classes of models are used in this study. One class of models is based on the electromagnetic laws governing the wave propagation. The other class describes the protonospheric and ionospheric plasma concentrations which affect the trajectories of VLF waves. Since the electromagnetic laws governing VLF propagation have been more fully explored than the physical laws governing the environment in which VLF waves propagate, we have concentrated on developing new, realistic models of the plasmasphere and have used standard, raytracing techniques to investigate magnetospheric duct propagation.

The first part of this report is a description of a protonospheric-ionospheric model used to simulate the diurnal and seasonal behavior of the magnetosphere. Special attention is given to the protonospheric-ionospheric interface. This is the region where enhancement ducts, which trap VLF waves in the magnetosphere, merge into the relatively uniform ionosphere. The altitude where this merging occurs defines the duct end-point height. Temporal variations in the height of the end-points of a magnetospheric duct affect the coupling between the earth's surface and the duct and the echoing properties of the duct. The relationship between $O^+ - H^+$ ion transition height and the end-points of magnetospheric ducts is described. The decay of a whistler duct due to thermal plasma flow is also discussed.

The second part of this report is a study of wave trapping properties of magnetospheric ducts. Rays are injected at the geomagnetic equator with a range in wave normal angles and positions inside a duct. The altitude where the rays leave the duct is a measure of the wave trapping efficiency.

FINAL REPORT ON
COMPUTER-AIDED SEMICON-
DUCTOR PROCESS MODELING
by J. D. Meindl, Director

University of Florida
Contract DAAB07-75-C-1344
from the ARPA
1 Jul 1975 - 30 Sep 1976

ABSTRACT

In military, industrial, commercial, and consumer applications, frequently there is a great necessity for "customizing" the design of an integrated circuit to fulfill the critical needs of a specific system or class of systems. A major barrier which prevents the economic production of small quantities of high performance custom integrated circuits is the cost of design. That is, the initial cost of designing optimum fabrication processes, device structures, and circuit configurations is prohibitively large because of the amount of empirical human effort which must be invested. The root cause of this problem is a glaring lack of adequate process, device, and circuit models and accompanying computer aided design techniques to ease the burden of custom design. Perhaps the most serious deficiency among these is the unavailability of suitable models for predicting accurately the physical characteristics of a monolithic structure on the basis of the control parameters for the corresponding fabrication processes. The salient objective of this program is the development of new basic models for integrated circuit processes which will permit accurate prediction of the characteristics of a monolithic structure on the basis of its proposed process parameters. These models will serve as the basis for economic computer aided design of optimum fabrication processes for custom integrated circuits.

The four key generic integrated circuit fabrication processes which are being investigated are (1) ion implantation, (2) thermal oxidation and chemical vapor deposition, (3) epitaxy, and (4) thermal diffusion. This report describes the progress which has been made in the first 15 months of this program in all four areas.

In ion implantation, studies have been done in two areas. Effects of implantation damage on impurity profiles in annealed Si have been investigated. A three-stream diffusion model for boron in silicon involving boron, vacancies and boron vacancy complexes has been proposed. The model is capable of predicting ordinary diffusion, proton enhanced diffusion and the annealing behavior of room-temperature implanted boron when appropriate restrictions on dose and annealing temperature are

obeyed. In the second study a straightforward approach to calculations of range profiles of dopant ions in multilayer media (e.g. arsenic implementation in silicon through a thin layer of silicon dioxide) has been developed based on numerical integration of the linearized Boltzmann transport equation. Using this approach, we have also calculated the range profiles of the recoiling ions which are knocked on from one layer of the substrate into the other layer by the projectiles (e.g. oxygen recoiling from SiO_2 into Si, by ions).

In the area of thermal oxidation and chemical vapor deposition the principal goal of the first year of the program has been to achieve accurate analytic prediction of oxide thickness for an arbitrary sequence of oxidations. At the present time, such prediction is possible only for lightly doped, (111) oriented silicon, with no chlorine species present during the oxidation process.

Toward this, kinetic oxidation data have been gathered under the following conditions:

- (a) Data for (111) and (100) silicon over the temperature range 700°C to 1200°C .
- (b) Data for dry O_2/HCl oxidation ambients containing 0-10% HCl for temperatures between 900°C and 1100°C .
- (c) Data for heavily phosphorous doped (111) substrates for surface concentrations up to solid solubility and temperatures between 900°C and 1100°C .

The availability of the above data now makes it possible to predict analytically the oxide thickness under a very wide range of ambient conditions and substrate orientation and doping levels.

In epitaxy, preliminary effort has been directed toward understanding the kinetics of growth and the mechanism of dopant incorporation in the epitaxial layer.

The dopant system of a horizontal silicon epitaxial reactor has been characterized by changing the dopant gas flow during the continuous deposition of epitaxial layers from silane. A system "transfer function" has been found relating the dopant profile in the epitaxial layer (system output) to the time-varying dopant gas flow (system input). The transfer

function allows the calculation of the dopant profile in the epitaxial film for any time varying dopant gas flow. The calculation of the dopant gas flow, as a function of the time required to achieve a desired dopant profile, is thus possible.

In thermal diffusion, a new mathematical model is being developed for the diffusion of impurities into silicon for both a constant source and drivein diffusion process. The model considers the influence of the internal electric field on the motion of impurity ions at elevated temperatures. The electric field is due to charge density produced by the ionization of impurities present in the material. Appendix B reviews the results of this study.

ERROR CORRECTION BY
ALTERNATE-DATA RETRY
by John J. Shedletsky

IBM Grad. Fellowship
NSF Grant GJ-40286
TR No. 113
May 1976

ABSTRACT

A new technique for low-cost error correction in computers is the alternate-data retry (ADR). An ADR is initiated by the detection of an error in the initial execution of an operation. The ADR is a re-execution of the operation, but with an alternate representation of the initial data. The choice of the alternate representation and the design of the processing circuits combine to insure that even an error due to a permanent fault is not repeated during retry. Error-correction is provided at a hardware cost comparable to that of a conventional retry capability.

Sufficient conditions are given for the design of circuits with an ADR capability. The application of an ADR capability to memory and to the data paths of a processor is illustrated.

ABSTRACT

In the well-known totally self-checking (TSC) network, a failure must not change one output codework into another. Called the fault-secure property, this permits a receiver of the net's output to assume that any codework it receives is correct. Further, the self-testing property requires that each possible failure in the net must produce at least one non-code output. Thus a receiver can monitor the health of the network by watching for non-code outputs.

In this paper we propose modifications of these two properties. The self-testing property is made more stringent. Each possible failure in the net is required to produce an output which is in a distinguished subset of the non-code outputs. The fault-secure requirement is modified to permit a fault to interchange certain output codewords. In particular, all outputs not in the distinguished subset are partitioned into equivalent classes, and a fault is permitted to change the output from one codeword to another codeword in the same class. However, a fault is not permitted to change the output from a codeword to any member of a different equivalence class (one not containing the correct output).

These modified properties define a generalization of the TSC network. A network which meets the modified properties is called a generalized self-checking (GSC) network. Self-checking and self-testing (Morphic) networks and TSC networks are special cases of the GSC network.

Examining TSC networks, we find a further connection with the GSC network. It has been known for some time that not every subnetwork of a TSC network need be TSC. We show that every subnetwork of a TSC network is GSC, and every TSC network is a cascade of GSC networks. This establishes the GSC network as the basic building block from which every TSC network is constructed.

We explore a brute-force method for constructing a desired TSC network by cascading GSC subnetworks. The method resorts to enumeration at many points of decision and thus is not a practical design tool. However, it does yield a very nice alternate realization of the Morphic OR, and suggests specializations which merit further study.

SYMMETRY, AUTOMORPHISM,
AND TEST
by André Verdillon

Inst. de Recherche en
Inf. et en Auto. Grant
NSF Grant MCS 76-05327
Tech. Note No. 87
June 1976

ABSTRACT

The study of regular structures such as tree, iterative, monotonic, functions has shown that by taking into account their properties the problem of finding a test can be reduced considerably. This paper shows how testing can be simplified by taking account symmetries that lead to network automorphisms. For an acyclic network of gates, methods are presented that give either an optimal or a near optimal test. It is shown how the concept of automorphism can be extended to networks of modules and how this allows using a multi-level description of a system.

ERROR MANAGEMENT
IN DIGITAL COMPUTER
INPUT/OUTPUT SYSTEMS
by Alan Michael Usas

NSF Fellow
NSF Grants
GJ-40286 and GK-43322
TR No. 122
May 1976

ABSTRACT

Historically peripheral devices have been more important in determining the market success of a computer system than the central processor. In spite of their key role the input/output (I/O) system components have been encumbered with a poor reputation for reliability and maintainability. To date there has been no comprehensive treatment of this problem. Presented here are techniques of error management (those steps taken to limit the effect of errors and to expedite recovery) appropriate for the buses, interfaces, controllers, and peripheral devices of the I/O system.

Many of the possible erroneous operations in an I/O system can be classified as either intolerable or tolerable on the basis of whether their effect is to physically damage a part of the system, such as a head "crash" on a disk drive, or cause some other irreversible action, or whether the error simply renders a device inoperable without destroying any information. Fail-safe circuits are designed to minimize the probability of just one of the two possible erroneous outputs from a single output circuit (i.e., erroneous 1 and 0), and thus represent a useful compromise solution over circuits that would reduce the likelihood of both types of errors. The design of fail-safe combinatorial circuits by use of asymmetrically failing components and circuit duplication is explored, and a new synthesis algorithm is presented. It is based on the probability of an unsafe erroneous output, which is a function of the input vectors and possible faults, rather than on just the probability of component failure. Fail-safe networks constructed using this algorithm will generally require less than complete duplication and will have a lower probability of intolerable erroneous outputs than if fault probabilities alone were considered. As sequential circuits are found throughout the interfaces and controllers of an I/O system, methods of constructing fail-safe versions that will not produce intolerable errors even after an erroneous state has been entered are explored. A straightforward design requiring at most two redundant state variables that explicitly traps the circuit in an erroneous state identified by

means of an error-detecting code is described and shown to be suitable for large-scale integration.

Besides the direct prevention of intolerable errors, the problem of detecting the occurrence of safe but nevertheless erroneous conditions is studied. To prevent checker or error detector failures from masking the indication of an erroneous condition, these circuits should fail to the error-indicating state. Designs for a variety of fail-safe checkers for velocity, position, timing, and other important peripheral device parameters that utilize the failure asymmetry of electro-optical components or duplication are described.

Specific modifications of magnetic disks, tapes, card readers and punches, line printers, and terminals using fail-safe circuits to reduce the probability of an intolerable error and checkers to enable timely error detection are detailed. A similar treatment is given to device controllers and interfaces with the further purpose of limiting the propagation of errors and that utilizes the controller to verify proper peripheral device operation.

A flexible maintenance bus is suggested as a solution to the problem of simplifying the human involvement with I/O system fault diagnosis. This bus, which is physically attached to a suspected faulty piece of equipment, acts like a programmable waveform generator and response recorder. It gives diagnostic programs access to a multiplicity of low level points in the I/O system not directly reachable by means of the standard I/O bus.

ABSTRACT

The pulse-echo imaging modality employed in medical acoustic imaging systems permits direct three-dimensional visualization of a reflecting object embedded in a three-dimensional acoustic medium (such as an organ in the interior of the human body). High resolution in range is achieved by range-gating ultrasonic pulses and, for the more advanced systems, high resolution in azimuth is achieved by focusing the sound with the aid of an array of acoustic transducers coupled to a system of controlled analog delay elements; the dynamic variation of these delay elements permits systematic exploration with the focused sound over the region of interest in the object space. In such a fashion, acoustic reflectivity is mapped into a brightness pattern (the image) on the face of a cathode ray tube.

Existing and proposed electronically-focused schemes of this kind are, with few exceptions, based on delay/sum processing of the detected acoustic signals; i.e., the outputs of the delay elements are coherently added together to yield one point in the image at a time. Until recently, most studies of focused, pulse-echo acoustic imaging systems have assumed that a steady-state (monochromatic) analysis was adequate to derive the essential characteristics of the system's performance, such as axial and lateral resolution and grating lobe properties. When very wideband pulses are employed (to achieve high depth resolution), however a more general wideband, temporal-spatial analysis of the system point response is required. For example, as the acoustic pulses become increasingly wideband, it is shown in this research that the lateral response of the (two-dimensional) temporal-spatial point spread function provided by simple delay/sum processing becomes increasingly poor. Here, a method is developed for restoring the degraded lateral response that takes place under very wideband conditions; this scheme is realized by a one-dimensional filtering operation performed on the output of the delay/sum stage of the basic imaging system. This leads to an improved overall axial-lateral (temporal-spatial) point spread function for the electronically-focused pulse-echo imaging system.

To develop the background for the study of wideband acoustic imaging systems, the theory of monochromatic scalar diffraction is extended to wideband disturbances. A variety of applications of the wideband theory is provided for illustration. Among these is a description of the wideband focusing of a plane wave impulse by a circular lens.

Following this, the subject of multiple-element focused array systems is developed. First, the monochromatic response of the focused system is derived; then, the theory of array focusing is extended to wideband operation. In particular, the wideband point response is obtained, and its dependence on the form of the temporal pulse is emphasized. Also, wideband grating-lobe behavior is investigated, and a convenient relative measure of comparison between the strength of the n^{th} grating lobe and the main lobe is derived.

Next, the general subject of wideband image reconstruction is developed, where delay/sum processing is evaluated and the axial-lateral resolution optimizing scheme is derived. Here, two possible reconstruction strategies are contrasted: coherent summation and deconvolution. It is shown that deconvolution provides the optimum wideband point response in the sense that an optimum compromise between axial and lateral resolution is automatically obtained, in contrast to coherent summation. The subject of wideband image reconstruction is concluded with the introduction of an alternative formulation of the problem of image reconstruction by deconvolution: an analytical inversion formula is derived that allows a function of reflectivity (the object) to be recovered from measurements of its line integrals defined over circular paths.

Finally, the subject of transmit/receive aperture synthesis is examined. A simple rule is derived which shows how a combination of two "incomplete" or sparse transmitting and receiving structures can be exploited to provide full aperture resolution. A variety of original examples is provided to illustrate this principle.

RESULTS OF AN INITIAL
ATTEMPT TO CRYPTANALYZE
THE NBS DATA ENCRYPTION
STANDARD

by M. Hellman, R. Merkle,
R. Schroepel, L. Washington,
W. Diffie, S. Pohlig,
P. Schweitzer

September 9, 1976
Revised:
November 10, 1976

ABSTRACT

The National Bureau of Standards has proposed a data encryption standard (DES) for nonmilitary governmental and commercial use. Such a cryptosystem can be used to provide both privacy and authentication to messages [1,2]. In many applications, authentication (a form of digital signature) is of primary interest.

For reasons of national security, NBS, IBM (which designed DES), and the National Security Agency (which participated in its evaluation), will not divulge the results of their tests concerning the strength of the system. Because they will also not explain the rationale behind certain critical elements or adequately quantify the level of security, we undertook an evaluation of DES in an attempt to determine its strengths and weaknesses. This evaluation lasted one month and involved approximately ten person weeks of effort. Our results are therefore only preliminary, and it must be assumed that an adversary with greater resources would make greater progress.

It is thus somewhat disturbing that we achieved a 50 percent savings in computation over an exhaustive search. We also found suspicious structure in the critical elements of the system (the S-boxes). This structure could be the result of an accidental weakness, a deliberately set trap door (i.e., hidden structure which allows those who know of it to break the system), or no weakness at all. An explanation and further study are needed before trust can be placed in DES. This need is enhanced because NSA does not want a genuinely strong system to frustrate its cryptanalytic intelligence operations. As a result, DES is mildly suspect a priori.

THE OPTIMAL PLACEMENT
OF DYNAMIC RECOVERY
CHECKPOINTS IN RECOV-
ERABLE COMPUTER SYSTEMS
by Wayne Alan Warren-Angelucci

DARPA Contract
MDA903-76C-0093
NSF Grant MC573-07973-A1,2
JSEP Contract
N00014-67-A-0112-0601
TR No. 126
December 1976

ABSTRACT

Reliability is an important concern of any computer system. No matter how carefully designed and constructed, computer systems fail. The rapid and systematic restoration of service after an error or malfunction is always a major design and operational goal. In order to overcome the effects of a failure, recovery must be performed to go from the failed state to an operational state. This thesis describes a recovery method which guarantees that a computer system, its associated data bases and communication transactions will be restored to an operational and consistent state within a given time and cost bound after the occurrence of a system failure.

This thesis considers the optimization of a specific software strategy - the rollback and recovery strategy, within the framework of a graph model of program flow which encompasses communication interfaces and data base transactions. Algorithms are developed which optimize the placement of dynamic recovery checkpoints. Presented is a method for statically pre-computing a set of optimal decision parameters for the associated program model, and a run-time technique for dynamically determining the optimal placement of program recovery checkpoints.

EQUIDENSITY ITOMETRY BY
COHERENT OPTICAL
FILTERING
by H. K. Liu, J. W.
Goodman, J. L-H. Chan

N00014-76-C-0514
TR No. 6415-8
October 1976

ABSTRACT

A new and simple method has been developed for fabrication of multilevel halftone screens that have proved useful for generation of equidensity contours by means of coherent optical filtering. Up to ten contours of constant brightness have been generated on a picture by coherent optical filtering of a single halftone copy of that picture. The possible application of this method to optical analog-to-digital conversion using a single halftone photograph is discussed.

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